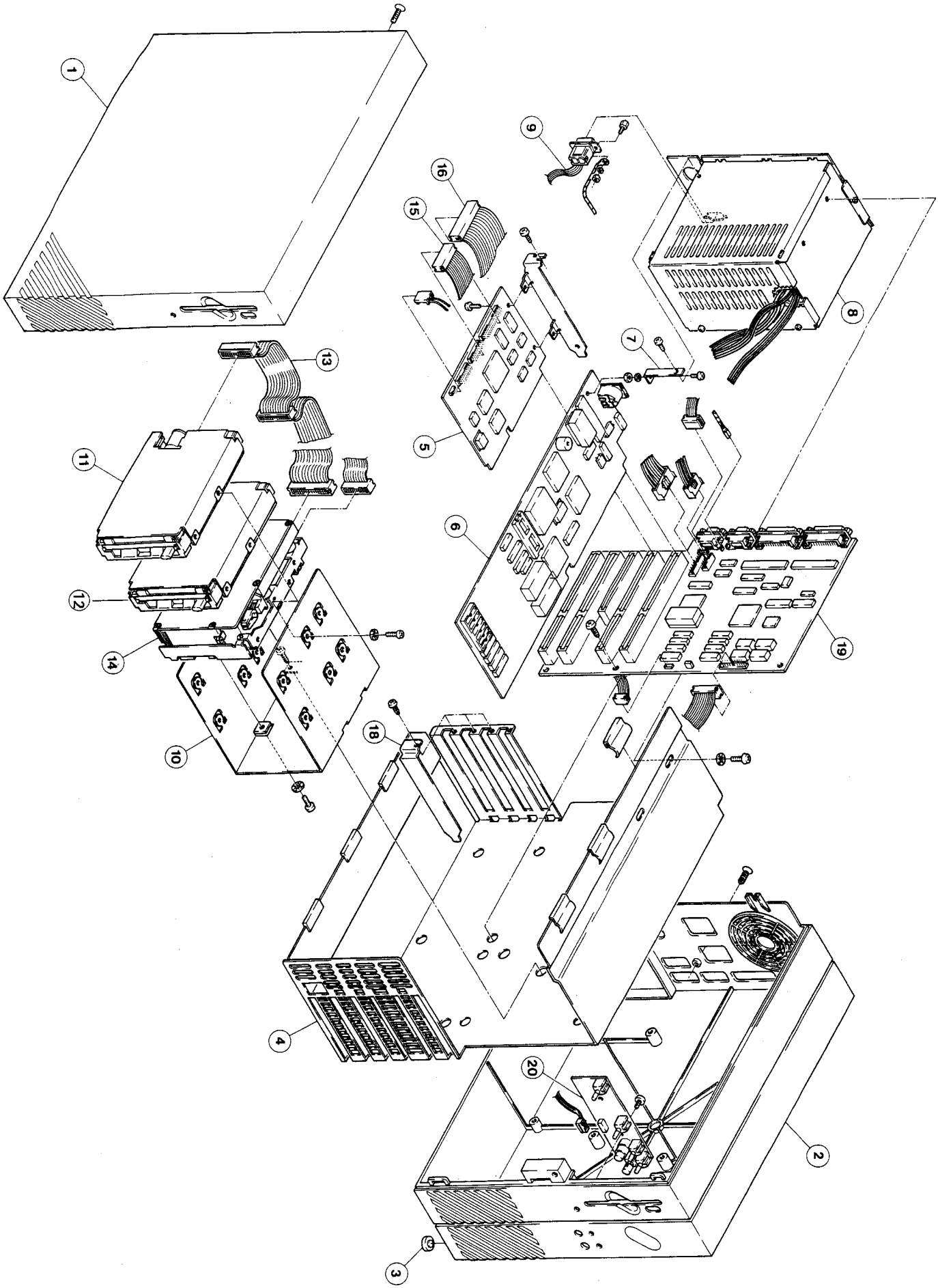
Kundendienst-Handbuch
Service Manual

Schneider

PERSONAL COMPUTER
386 SX

386 SX, System 40
386 SX, System 70

Exploded view



Ersatzteilliste für 386 SX, System 40
Parts List for 386 SX, System 40

Bestell-Nr. Part.-No.	Bezeichnung	Description	Zeich.-Pos. Ref.-No.	Preisgruppe
51 130 00	FK System 386 SX	Box system 386 SX		C 3
50 466 00	Sty-Verp. System 386 SX	Polyfoam system 386 SX		C 3
50 495 00	FK Tastatur 386 SX	Box keyboard 386 SX		C 2
50 496 00	Sty-Verp. Tastatur 386 SX	Polyfoam keyboard 386 SX		C 2
52 271 00	Tastatur (D)	Keyboard (D)		F 6
50 482 00	Tastatur (F)	Keyboard (F)		F 6
50 202 00	Tastatur (DK)	Keyboard (DK)		F 6
50 203 00	Tastatur (I)	Keyboard (I)		F 6
50 204 00	Tastatur (N)	Keyboard (N)		F 6
50 485 00	Tastatur (S/SF)	Keyboard (S/SF)		F 6
50 206 00	Tastatur (P)	Keyboard (P)		F 6
50 214 00	Tastatur (GR)	Keyboard (GR)		F 6
50 484 00	Tastatur (GB)	Keyboard (GB)		F 6
50 483 00	Tastatur (E)	Keyboard (E)		F 6
50 486 00	Tastatur (CH)	Keyboard (CH)		F 6
50 097 00	Netzkabel (D)	Cord AC (D)		C 0
50 562 00	Netzkabel (GB)	Cord AC (GB)		C 0
50 617 00	Netzkabel (CH)	Cord AC (CH)		C 0
50 225 00	Gehäuse Oberteil	Cabinet top	1	C 3
50 226 00	Gehäuse Unterteil	Cabinet bottom	2	C 9
50 493 00	Gehäusefuß	Leg	3	A 5
52 172 00	Blechchassis	Chassis metal	4	D 4
52 482 00	Platine Best. (D) CPU 386 SX	PCB (D) CPU 386 SX	6	*
50 293 00	Haltewinkel CPU Leiterplatte	Angle CPU	7	A 9
52 477 00	Netzteil 90 W	Power supply 90 W	8	G 8
50 448 00	Kabelbaum 9pol.	Cable 9-pin	9	B 8
50 171 00	Floppyhalter	Bracket floppy	10	B 8
50 021 00	Floppy-Laufwerk	Floppy disk drive	11	G 0
50 472 00	Floppy-Laufwerk	Floppy disk drive	12	F 8
50 221 00	Kabelbaum Floppy 26pol.	Cable floppy 26-pin	13	B 7
50 550 00	Hard Disk Laufwerk 40 MB	Hard disk drive 40 MB	14	*
51 444 00	HD-Kabel	Cable HD	16	C 0
50 224 00	Blindblende	Plate blind	17	A 9
50 020 00	Blindblech	Plate blind	18	B 9
50 925 00	Platine Best. (D) VGA I/0	PCB (D) VGA I/0	19	J 5
51 534 00	Platine Best. LED-Panel	PCB LED-Panel	20	C 7
50 056 00	Druckknopf für FDD (Toshiba)	Push-button FDD (Toshiba)		A 5
50 294 00	Druckknopf für FDD (Sony)	Push-button FDD (Sony)		A 5
51 458 00	Adapterkabel HD, 4pol.	Cable, HD 4-pin		B 4
51 447 00	Kabelbaum LED-Panel	Cable, LED-Panel		B 3
51 274 00	Abschirmblech	Shielding		C 6

Ersatzteilliste für 386 SX, System 70
Parts List for 386 SX, System 70

Bestell-Nr. Part.-No.	Bezeichnung	Description	Zeich.-Pos. Ref.-No.	Preisgruppe
50 502 00	HD-Controller	HD-Controller	5	G 7
52 474 00	Haltewinkel HD-Controller	Angle, HD-Controller		B 3
50 469 00	Hard Disk Laufwerk 60 MB	Hard disk drive 60 MB	14	*
52 476 00	Kabelbaum HD-Contr. I/0 Pl.	Cable HD-Contr. I/0 Board		C 5
50 220 00	Kabelbaum 20pol.	Cable 20-pin	15	B 9
50 223 00	Kabelbaum 34pol.	Cable 34-pin	16	C 5

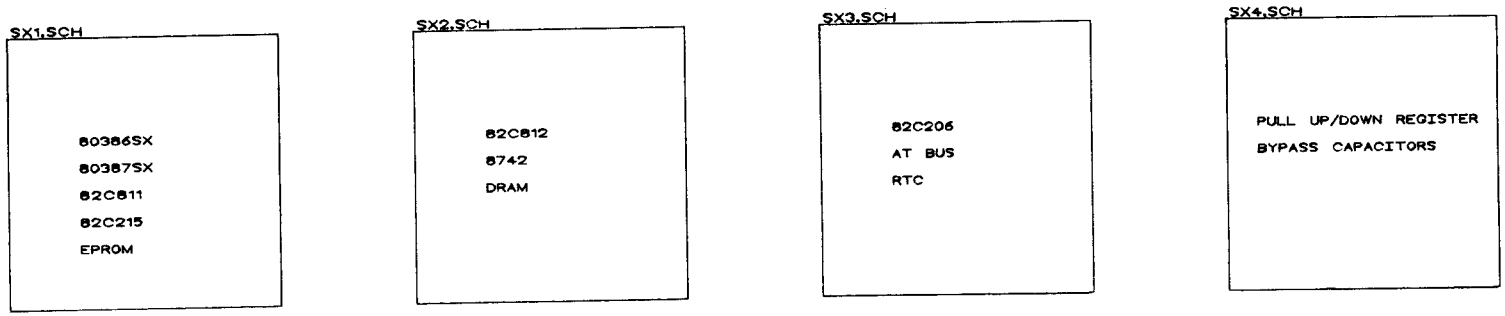
Note: All spare parts with countryindex are reserved for foreign distributors only.

All 3.5″ and 5.25″ floppydisks must be replaced by new ones. Schneider passes no exchange price to the distributor or dealer.

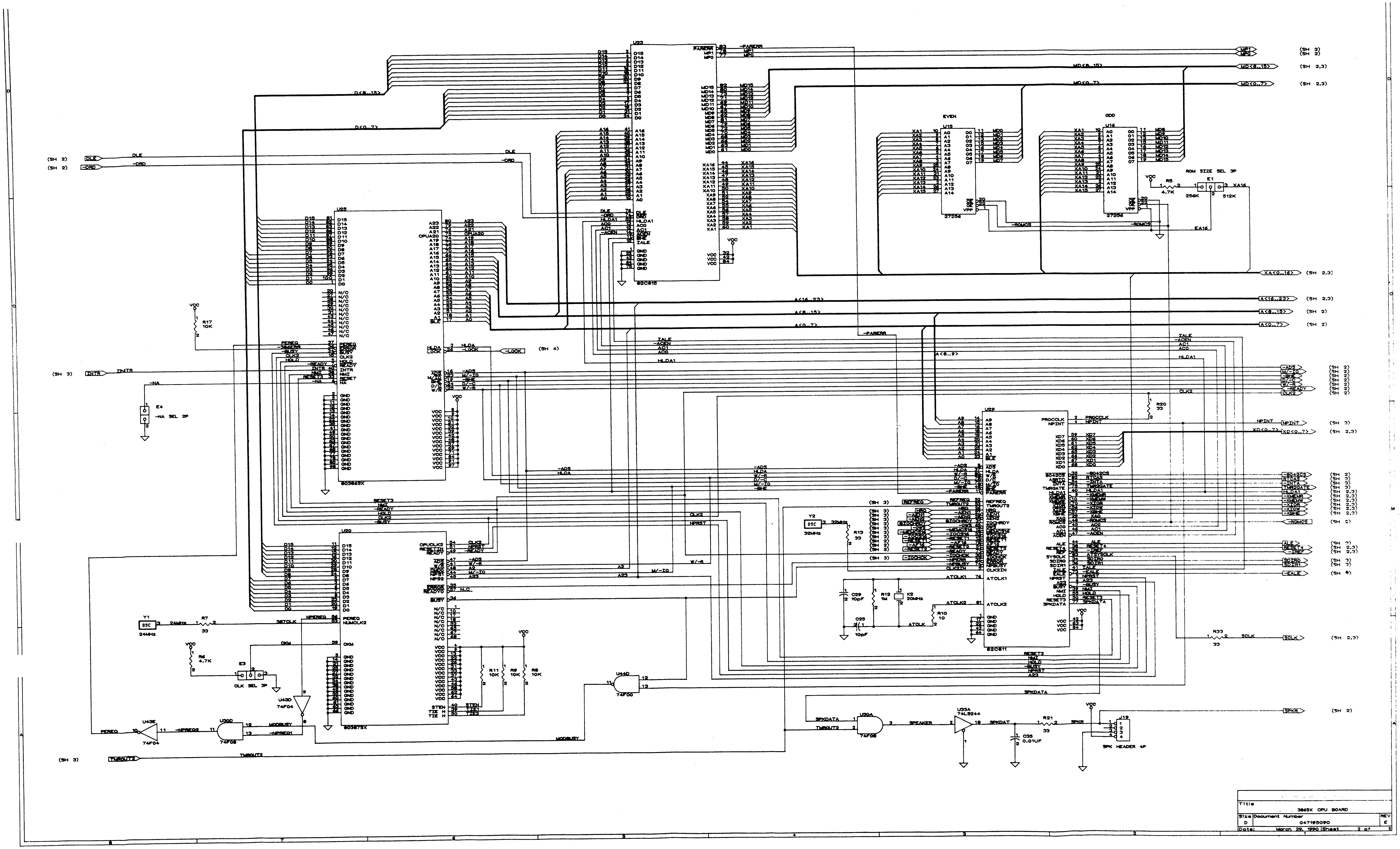
*Preis auf Anfrage

* Please call for price

386SX CPU BOARD CIRCUIT DIAGRAM



Title: 386SX CPU BOARD		
Size: B	Document Number: 047195090	REV: E
Date: March 29, 1990	Sheet: 1 of 5	


U23
82C815
U25
80386SX
U20
80387SX
U29
82C611
EVEN
U15
27256
ODD
U16
27256
ROM SIZE SEL 3P
E1
256K
512K
R5
4.7K
E4
-NA SEL 2P
R17
10K
Y1
OSC
24MHz
R7
33
R6
4.7K
E3
CLK SEL 3P
U43D
74F04
U43E
74F04
U30D
74F08
U44D
74F00
R11
10K
R9
10K
R8
10K
Y2
OSC
32MHz
R13
33
C29
10pF
R12
1M
X2
20MHz
C25
10pF
R10
10
R20
33
R33
33
SCLK
U30A
74F08
SPEAKER
U33A
74LS244
SPKDAT
C35
0.01UF
R21
33
SPKR
J19
SPK HEADER 4P
D<8..15>
D<0..7>
MD<8..15>
MD<0..7>
XA<0..16>
A<16..23>
A<8..15>
A<0..7>
XD<0..7>
TMROUT2
Title
386SX CPU BOARD
Size
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Document Number
047195090
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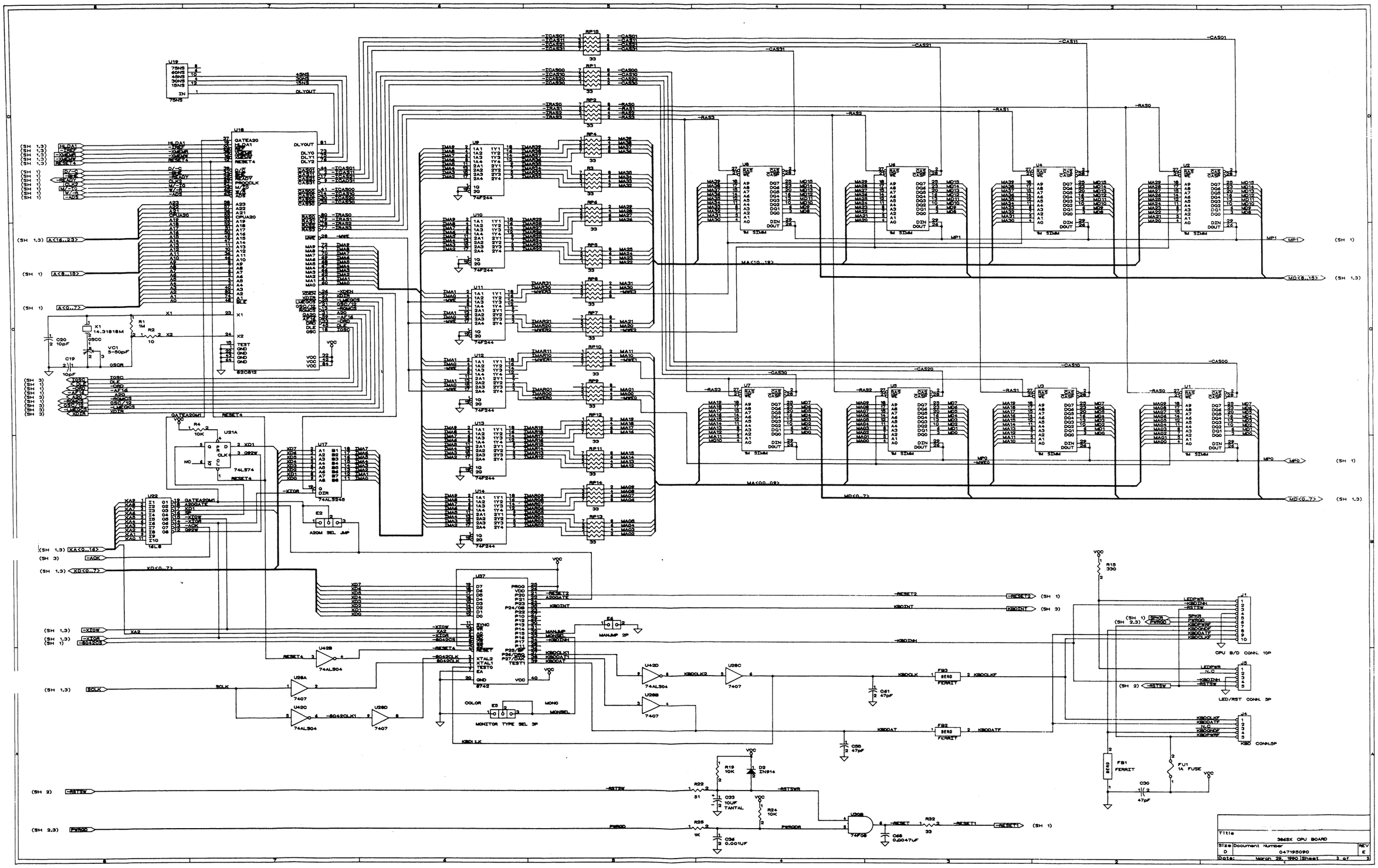
Date:
March 29, 1990
Sheet
2 of 5


U19
74AS8
40MS
40MS8
32MS
16MS
IN
75MS
DLYOUT
U18
GATEA20
HLDA1
-HOLD
-SMIRQ
-SMIWR
-RESET4
RESET4
D/-C
R/-C
-MEMCS
-IOCS
-MEMR
-MEMW
-IOR
-IOW
-ADS
CLK
A23
A22
A21
CPUA20
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
BHE
X1
X2
OSCI
OSCR
VCC
GND
82C812
(SH 1,3) A<16..23>
(SH 1) A<8..15>
(SH 1) A<0..7>
C20 10pF
C19 10pF
X1 14.31818M
R1 1M
R2 10
VC1 5-50pF
RESET4
GATEA20M
R4 10K
U21A
74LS74
XD1
-XIOW
-XIOR
-ADS
Q82W
U17
74ALS245
-XIOR
E2
A20M SEL JMP
U22
16L8
GATEA20M
A20GATE
XD1
-XIOW
-XIOR
-ADS
Q82W
(SH 1,3) XA<0..16>
(SH 3) -ACK
(SH 1,3) XD<0..7>
XD<0..7>
U9
U10
U11
U12
U13
U14
74F244
RP15
RP1
RP2
RP3
RP4
RP5
RP6
RP7
RP8
RP9
RP10
RP11
RP12
RP13
RP14
33
-CAS31
-CAS21
-CAS11
-CAS01
-CAS30
-CAS20
-CAS10
-CAS00
-RAS3
-RAS2
-RAS1
-RAS0
U8
U6
U4
U2
U7
U5
U3
U1
1M STIMM
MP1
MP0
-MWE0
MA<00..09>
MD<0..7>
(SH 1)
(SH 1,3)
U37
8742
-RESET2
A20GATE
KBDINT
MANJMP
-KBDINH
KBDCLK1
KBDDAT1
P20
P21
P22
P23
P24/P08
P25/P09
P26/P10
P27/P11/BAK
P12
P13
P14
P15
P16
P17
P10
P11
TEST0
TEST1
EA
XTAL2
XTAL1
SYNC
RESET
E4
MANJMP 2P
U42B
74ALS04
U42D
U28C
7407
U28A
U42C
U28D
U28B
-8042CS
-8042CLK
-8042CLK1
-RESET4
XA2
-XIOW
-XIOR
SCLK
COLOR
MONO
MONSEL
E5
MONITOR TYPE SEL 3P
KBDCLK2
KBDCLK
KBDDAT
FB3
FB2
FERRIT
C61 47pF
C58 47pF
R12 330
J1
CPU B/D CONN. 10P
J5
LED/RST CONN. 5P
J4
KBD CONN.5P
LEDPWR
-KBDINH
-RSTSW
SPKR
PWR0D
KBDPWRF
KBDCNCF
KBDDATF
KBDCLKF
N.C
FB1
FERRIT
FU1
1A FUSE
C30 47pF
R19 10K
D2 1N914
R22 51
C33 10UF TANTAL
R24 10K
R25 1K
C36 0.001UF
U20B
74F08
R32 33
C68 0.0047uF
-RSTSWR
PWR0DR
-RESET1
(SH 1)
(SH 2)
(SH 2,3)
Title
386SX CPU BOARD
Size
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Document Number
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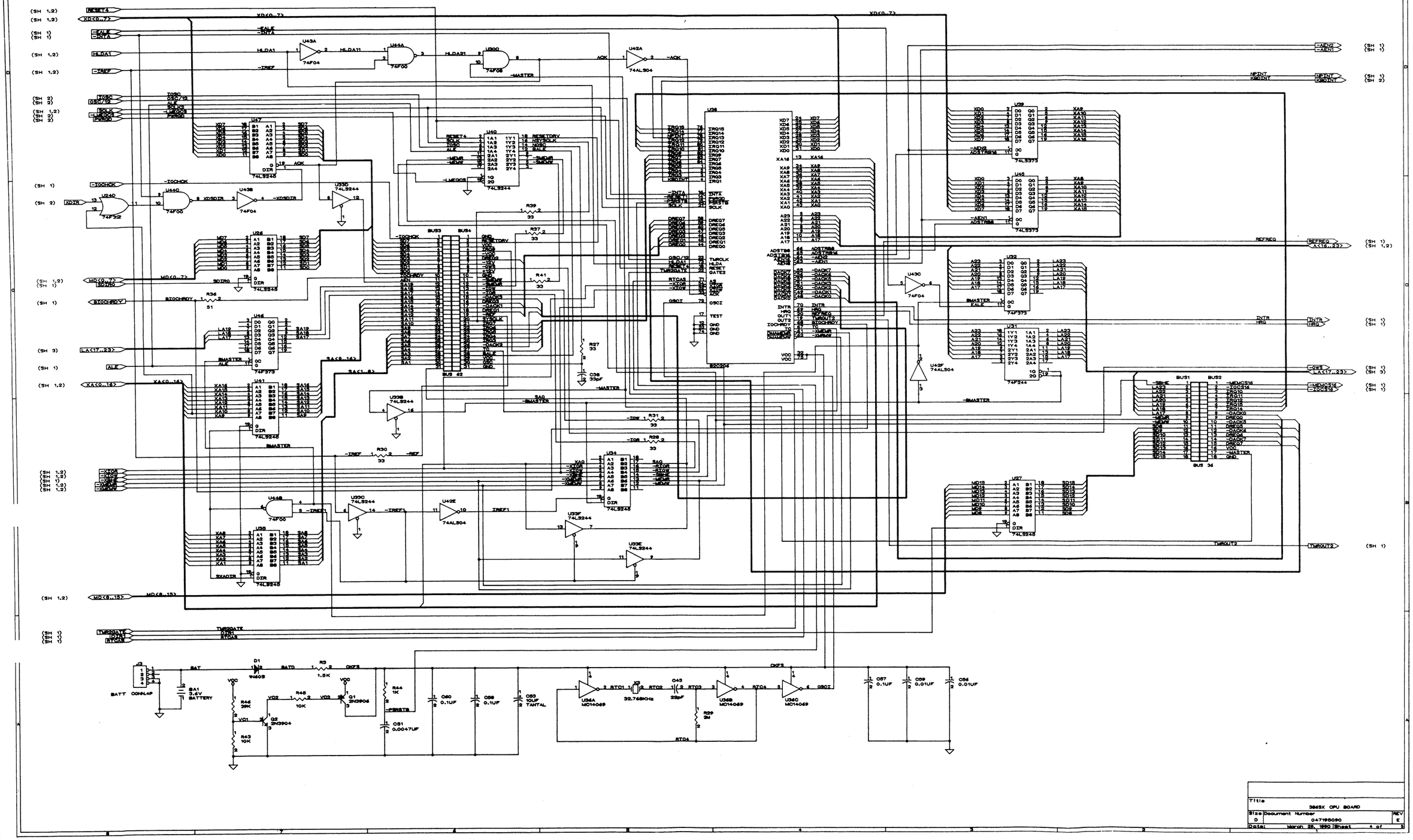
Date:
March 29, 1990
Sheet
3 of 5


RESET4
XD<0..7>
-EALE
-INTA
HLDA1
-INREF
U43A
74F04
HLDA11
U44A
74F00
HLDA21
U30D
74F08
-MASTER
ACK
U42A
74ALS04
-ACK
U38
82C304
U47
74LS245
U40
74LS244
U44D
74F00
U43B
74F04
U33D
74LS244
-IOCHCK
XDDIR
U24D
74F32
-XDSDIR
R39
33
R37
33
R41
33
U26
74LS245
MD<0..7>
SDDIR
-IOCHRDY
R36
51
U46
74F373
LA<17..23>
ALE
BMASTER
XA<0..16>
U41
74LS245
R27
33
C38
330pF
U33B
74LS244
R31
33
R28
33
R30
33
-INREF
-REF
U34
74LS245
RA9
-RTCR
-IOW
-IOR
-MEMR
-MEMW
U48B
74F00
-INREF1
U33G
74LS244
U42E
74ALS04
INREF1
U38
74LS245
SA<0..16>
SAADIR
MD<8..15>
U33F
74LS244
U33E
74LS244
U43C
74F04
U42F
74ALS04
U32
74F373
U31
74F244
U45
74LS373
U39
74LS373
-AEN2
-AEN1
NEXINT
XMOINT
REFREQ
INTR
IRQ
-OWS
-MEMCS16
-IOCS16
BUS1
BUS2
BUS 36
U27
74LS245
TMROUT2
BATT CONN4P
J3
BAT
D1
1N4003
BATD
R5
1.5K
CKFS
SA1
3.6V
BATTERY
VCC
R44
1K
PRESETB
C61
0.0047UF
C60
0.1UF
C58
0.1UF
C63
10UF
TANTAL
R46
39K
VC1
VC2
R45
10K
VC3
Q1
2N3906
Q2
2N3904
R43
10K
U36A
MC14069
X3
32.768KHz
C43
22pF
U36B
MC14069
R29
2M
RTC4
U36C
MC14069
C57
0.1UF
C59
0.01UF
C56
0.01UF
Title
386SX CPU BOARD
Size
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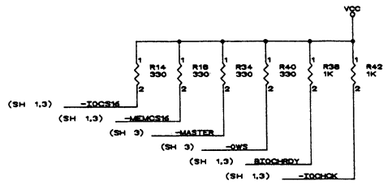
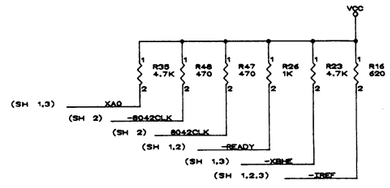
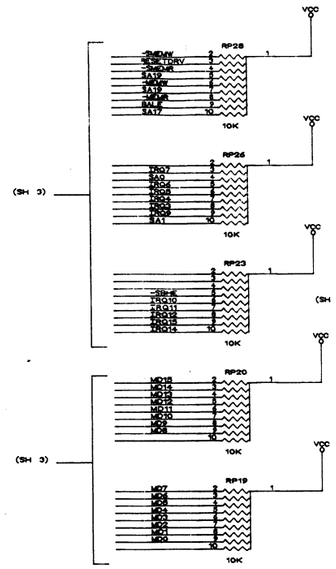
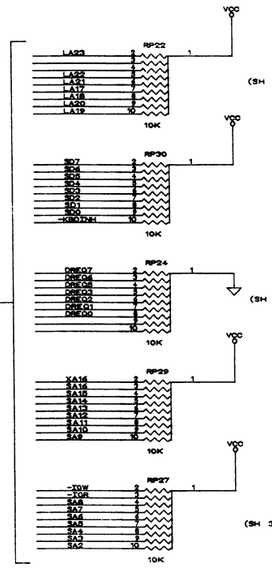
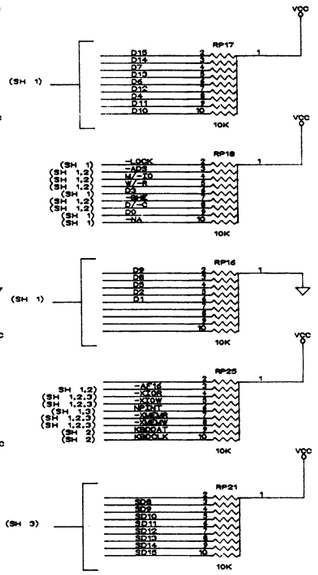
Document Number
04719S090
REV
E
Date:
March 22, 1990
Sheet
4 of
5

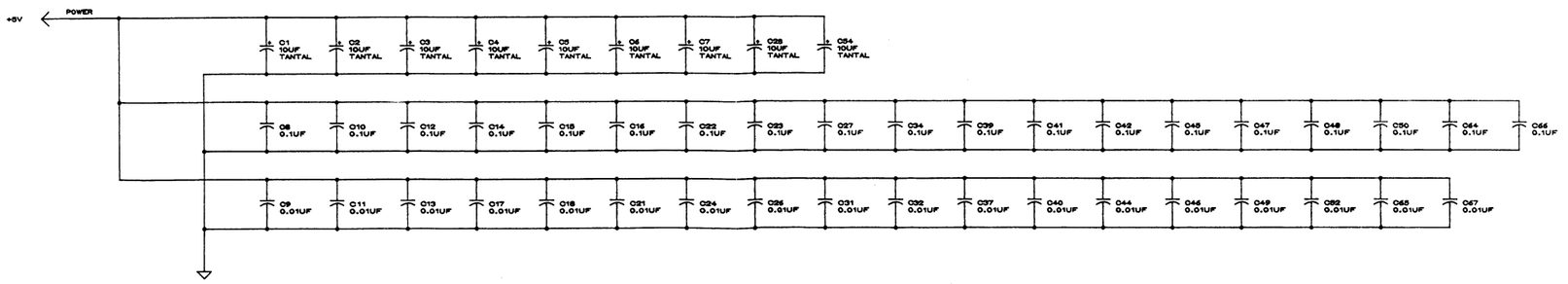






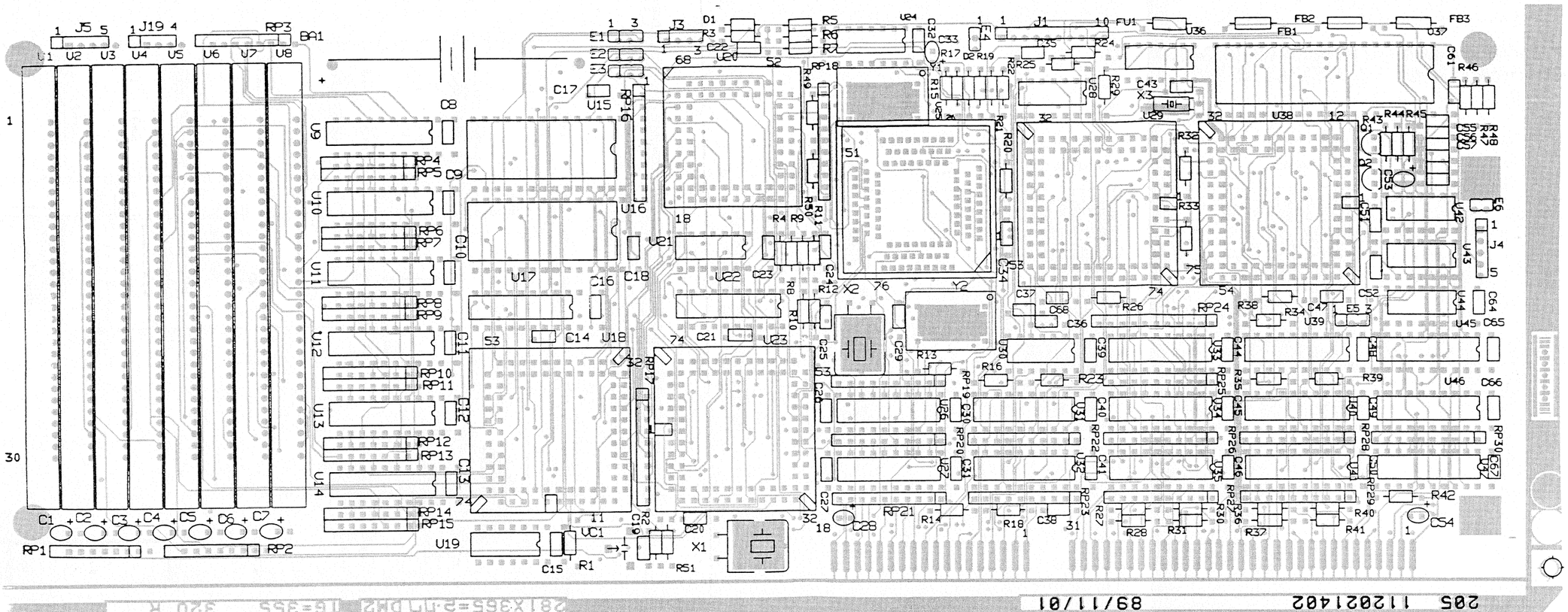




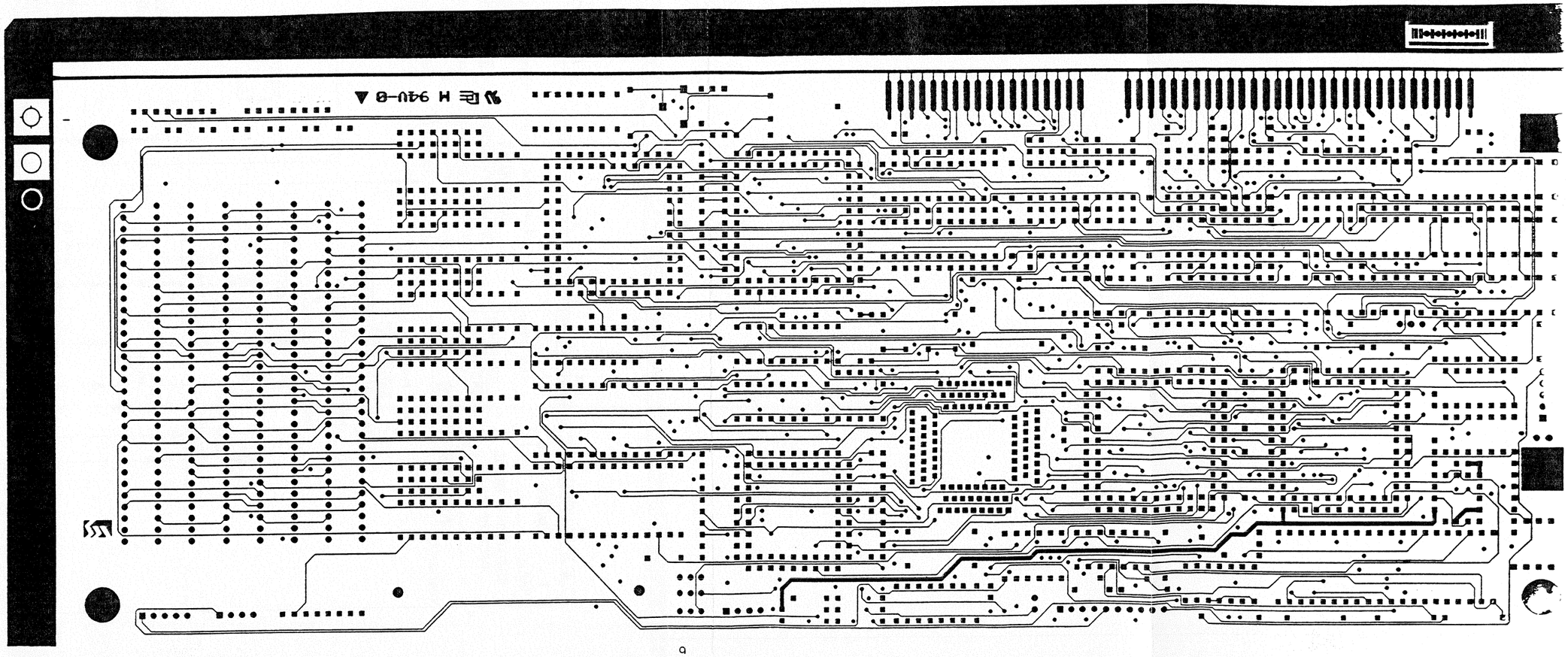


Title: 386SX CPU BOARD		
Size: D	Document Number: 047195090	REV: E
Date: March 29, 1990	Sheet 8 of 8	

CPU
Component side

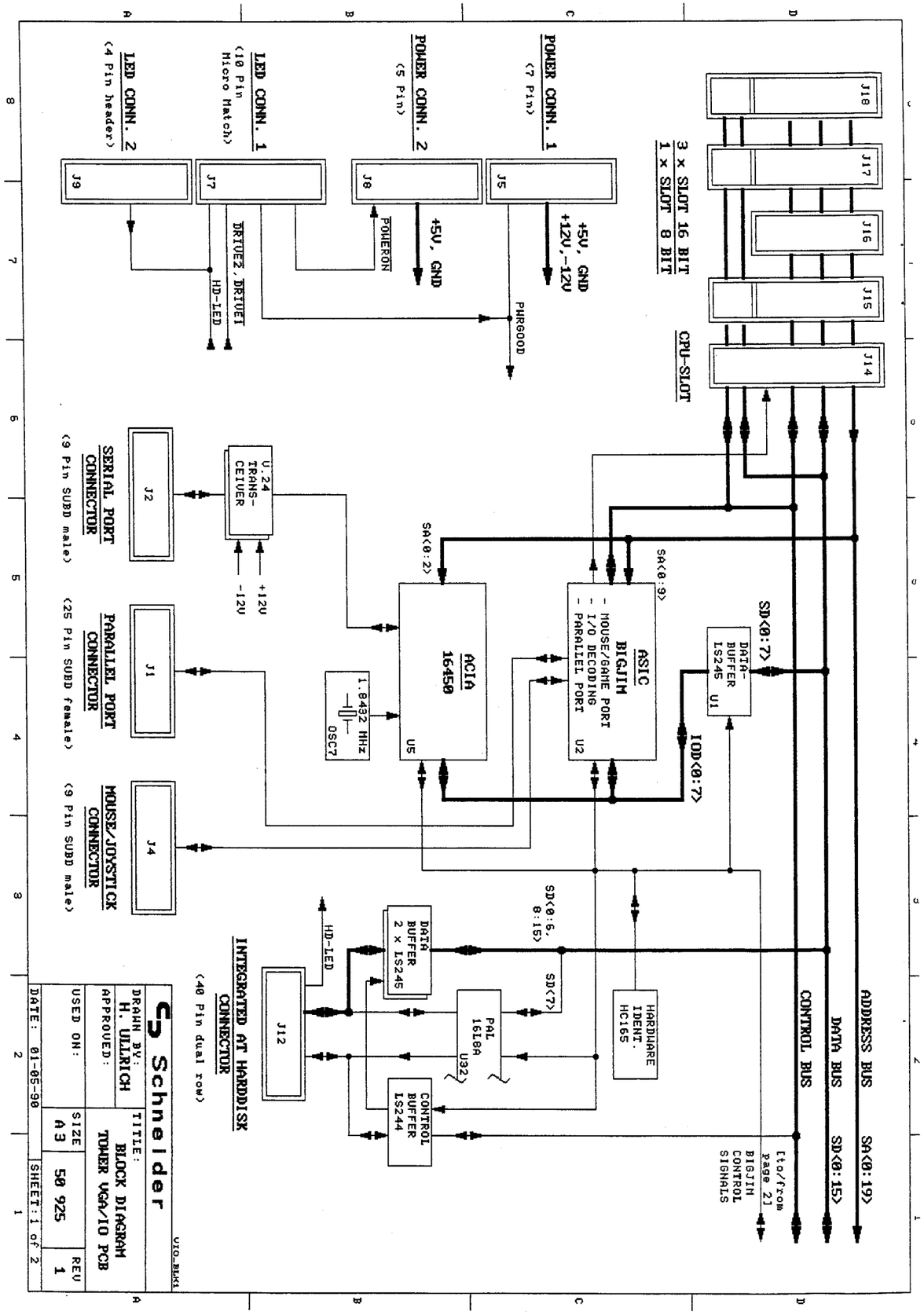


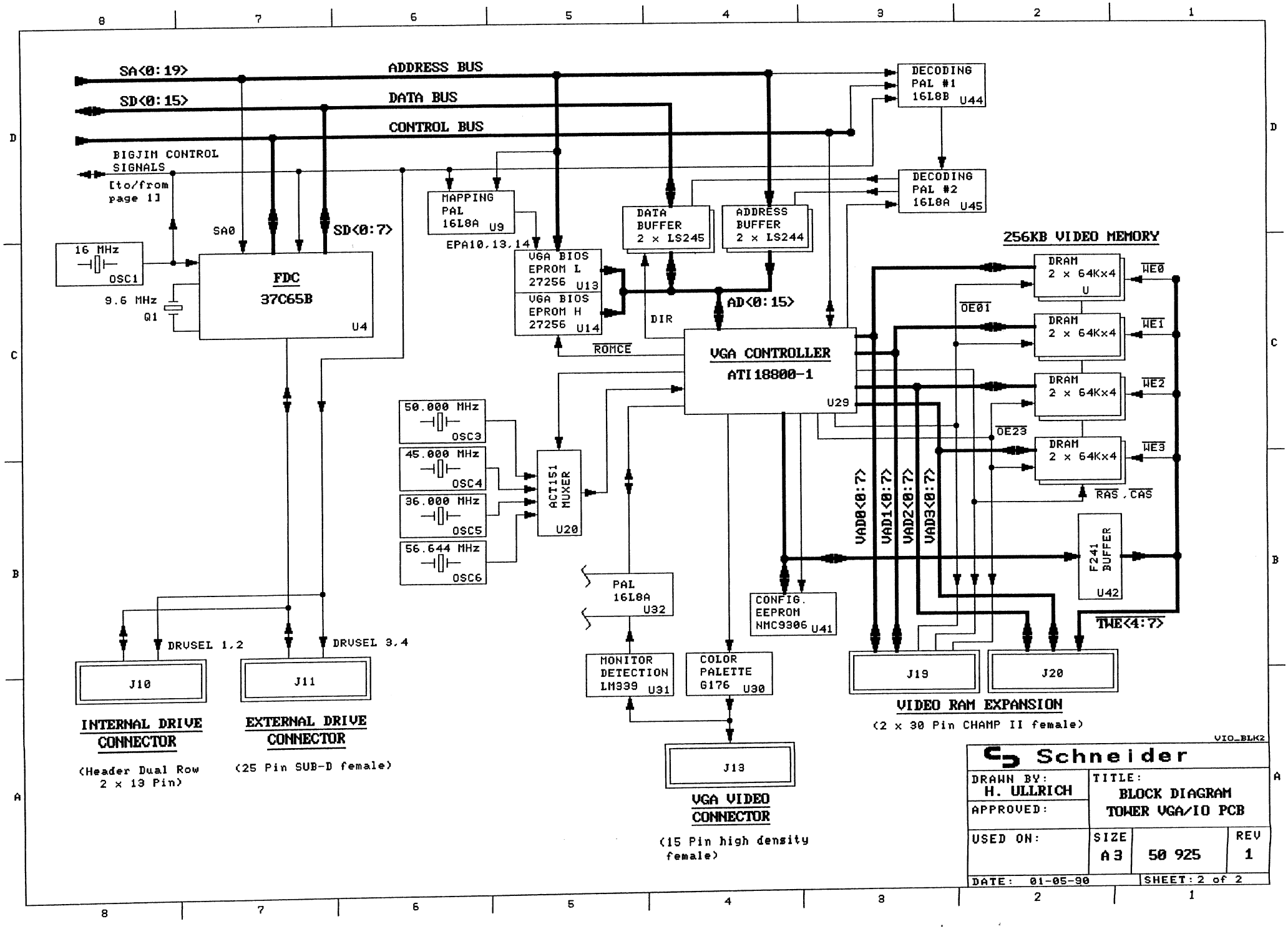
Soldering side



Ersatzteilliste für Platine Best. (D) 386 SX CPU
Parts List for P.C.B. (D) 386 SX CPU

Bestell-Nr. Part.-No.	Bezeichnung	Description	Zeich.-Pos. Ref.-No.	Preisgruppe
52 504 00	IC 27256-25 BIOS „LOW“	IC 27256-25 BIOS “LOW”	U 15	D 0
52 505 00	IC 27256-25 BIOS „HIGH“	IC 27256-25 BIOS “HIGH”	U 17	D 0
60 189 00	IC 82 C 812-16	IC 82 C 812-16	U 18	E 6
60 190 00	IC 82 C 215-16	IC 82 C 215-16	U 23	D 6
52 850 00	IC 80 386 SX-16 MHz	IC 80 386 SX-16 MHz	U 25	H 1
60 191 00	IC 82 C 811-16	IC 82 C 811-16	U 29	E 6
60 192 00	IC 82 C 296	IC 82 C 296	U 38	E 8
50 907 00	RAM-Modul 1 MB × 9 100 nS	RAM Module 1 MB × 9 100 nS		G 3
50 325 00	Quarz 14,31818 MHz	Crystal 14.31818 MHz	X 1	B 3
60 193 00	Quarz 20 MHz	Crystal 20 MHz	X 2	B 0
44 673 00	Quarz 32,768 kHz	Crystal 32.768 kHz	X 3	A 7
50 315 00	Oszillator 24 MHz	Oscillator 24 MHz	Y 1	C 0
50 833 00	Oszillator 32 MHz	Oscillator 32 MHz	Y 2	B 8
60 194 00	Batterie 3,6 V	Battery 3.6 V	BA 1	C 5
50 332 00	Summer	Buzzer	J 19	A 8





VIO_BLK2

Schneider

DRAWN BY: H. ULLRICH	TITLE: BLOCK DIAGRAM TOWER VGA/IO PCB	
APPROVED:		
USED ON:	SIZE A3 / 50 925	REV 1
DATE: 01-05-90	SHEET: 2 of 2	

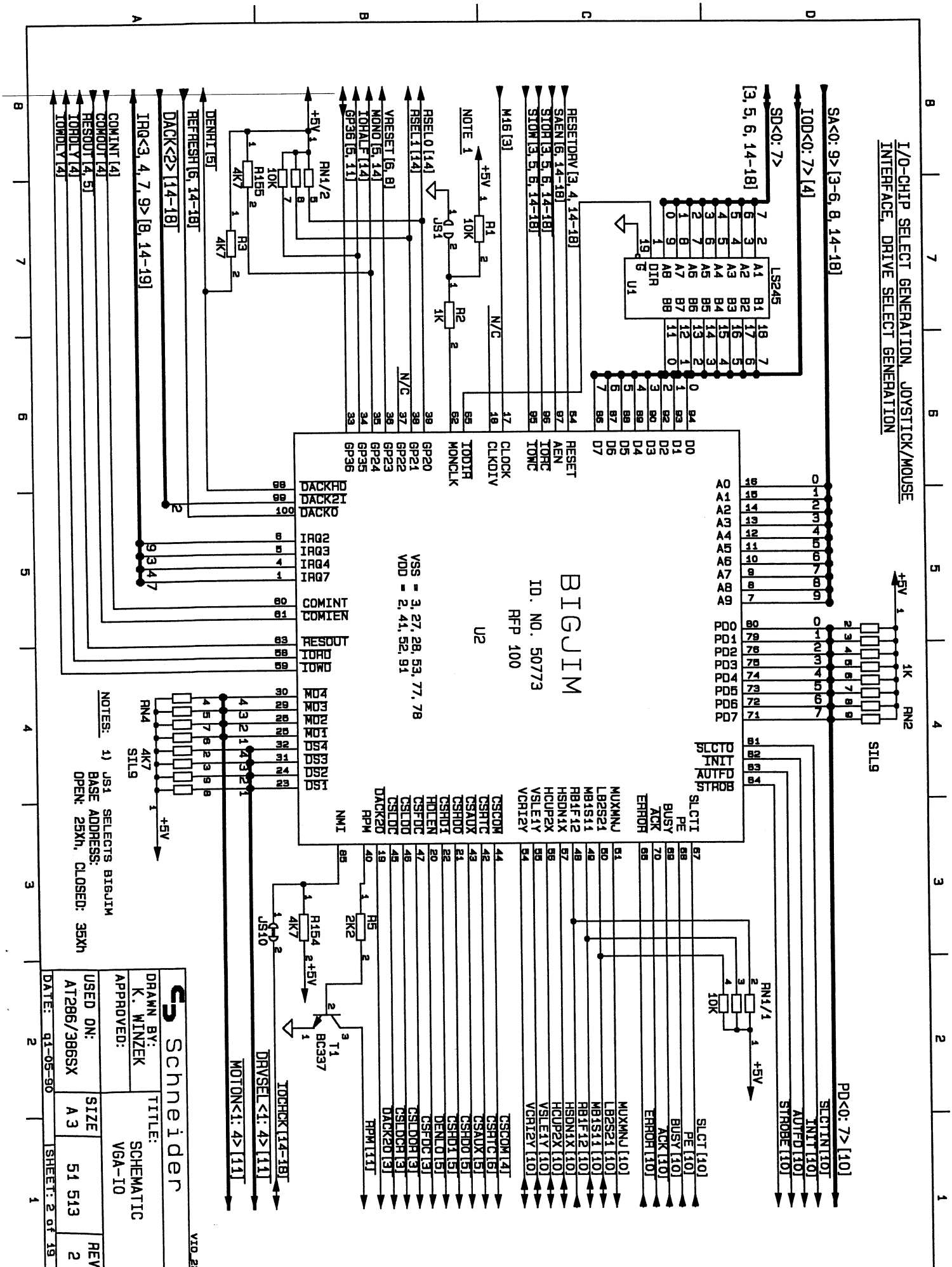
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
1	ADVANCED ENGINEERING RELEASE	07-17-89	
2	NEW RAM MODUL CONNECTORS, DIODE D6 ADDED (PCB REV.2 AND REV.1A)	01-08-90	K. WINZEK

DRAWING FILES:	CONTENTS:
VIO_21.DWG	THIS SHEET
VIO_22.DWG	ASIC BIGJIM
VIO_23.DWG	FLOPPY INTERFACE
VIO_24.DWG	SERIAL INTERFACE
VIO_25.DWG	INTEGRATED DRIVE INTERFACE
VIO_26.DWG	VIDEO I (BUS INTERFACE & ROM)
VIO_27.DWG	VIDEO II (CLOCK GENERATION)
VIO_28.DWG	VIDEO III (CONTROLLER)
VIO_29.DWG	VIDEO RAM
VIO_210.DWG	CONNECTORS I
VIO_211.DWG	CONNECTORS II
VIO_212.DWG	CONNECTORS III
VIO_213.DWG	CONNECTORS IV
VIO_214.DWG	CPU SLOT
VIO_215.DWG	NORMAL SLOT
VIO_216.DWG	NORMAL SLOT
VIO_217.DWG	NORMAL SLOT
VIO_218.DWG	NORMAL SLOT
VIO_219.DWG	BLOCK CAPS, SPARE GATES

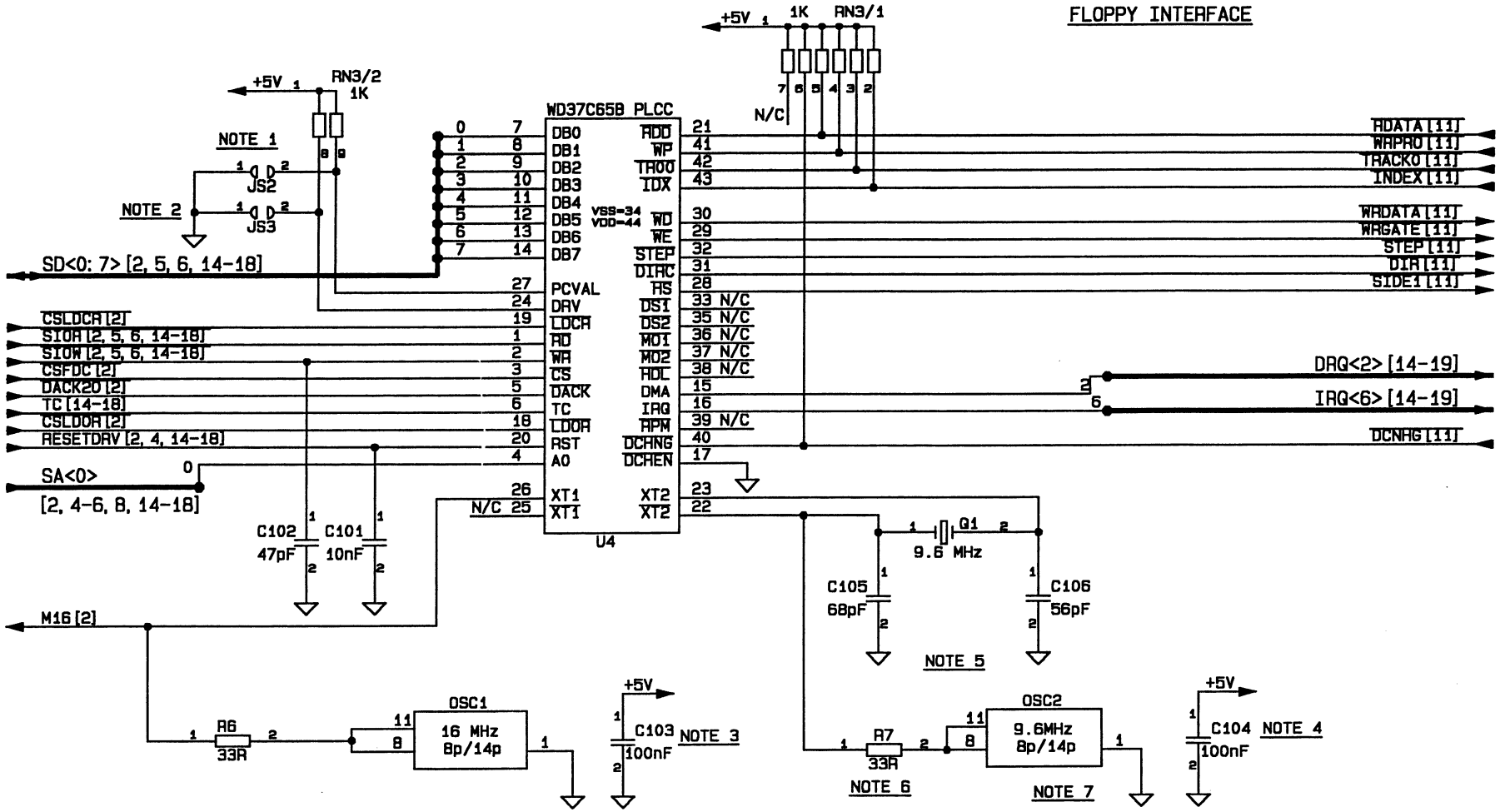
VIO_21

Schneider

DRAWN BY: K. WINZEK	TITLE: SCHEMATIC TOWER-VGA/IO		
APPROVED:			
USED ON: AT286/386SX	SIZE A 3	50 925	REV 2
DATE: 01-08-90	SHEET: 1 of 19		


I/O-CHIP SELECT GENERATION, JOYSTICK/MOUSE INTERFACE, DRIVE SELECT GENERATION
BIGJIM
ID. NO. 50773
RFP 100
U2
VSS = 3, 27, 28, 53, 77, 78
VDD = 2, 41, 52, 91
SA<0:9> [3-6, 8, 14-18]
IOD<0:7> [4]
SD<0:7>
[3, 5, 6, 14-18]
LS245
U1
DIR
RESETDRV [3, 4, 14-18]
SAEN [6, 14-18]
SIOR [3, 5, 6, 14-18]
SIOW [3, 5, 6, 14-18]
M16 [3]
NOTE 1
N/C
JS1
R1 10K
R2 1K
RN1/2 10K
R155 10K
R3 4K7
RSEL0 [14]
RSEL1 [14]
VRESET [6, 8]
MONO [5, 14]
IOHALF [14]
GP36 [5, 11]
DENRI [5]
REFRESH [6, 14-18]
DACK<2> [14-18]
IRQ<3, 4, 7, 9> [8, 14-19]
COMINT [4]
COMOUT [4]
RESOUT [4, 5]
IORDLY [4]
IOWDLY [4]
RESET
AEN
IORC
IOWC
CLOCK
CLKDIV
IODIR
MONCLK
GP20
GP21
GP22
GP23
GP24
GP35
GP36
D0
D1
D2
D3
D4
D5
D6
D7
DACKRQ
DACK2I
DACK0
IRQ2
IRQ3
IRQ4
IRQ7
COMINT
COMIEN
RESOUT
IORD
IOWD
MD4
MD3
MD2
MD1
MD0
DS4
DS3
DS2
DS1
NMI
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
SLCTP
INITP
AUTFDP
STROBP
SLCTI
PE
BUSY
ACK
ERROR
MUXMNJ
LB2S21
MB1S11
RB1F12
HSDN1X
HCUP2X
VSLE1Y
VCRI2Y
CSCOM
CSATC
CSAUX
CSRD0
CSRD1
DENLO
CSFDC
CSLDDR
CSLDCR
DACK20
RPM
RN2 1K SIL9
RN1/1 10K
PD<0:7> [10]
SLCTIN [10]
INIT [10]
AUTFD [10]
STROBE [10]
SLCT [10]
PE [10]
BUSY [10]
ACK [10]
ERROR [10]
MUXMNJ [10]
LB2S21 [10]
MB1S11 [10]
RB1F12 [10]
HSDN1X [10]
HCUP2X [10]
VSLE1Y [10]
VCRI2Y [10]
CSCOM [4]
CSATC [6]
CSAUX [5]
CSRD0 [5]
CSRD1 [5]
DENLO [5]
CSFDC [3]
CSLDDR [3]
CSLDCR [3]
DACK20 [3]
RPM [11]
IOCHCK [14-18]
DRVSEL<1:4> [11]
MOTON<1:4> [11]
RN4 4K7 SIL9
R154 4K7
R5 2K2
JS10
T1 BC337
NOTES: 1) JS1 SELECTS BIGJIM BASE ADDRESS: OPEN: 25Xh, CLOSED: 35Xh
Schneider
DRAWN BY: K. WINZEK
APPROVED:
TITLE: SCHEMATIC VGA-IO
USED ON: AT286/386SX
SIZE A 3
51 513
REV 2
DATE: 01-05-90
SHEET: 2 of 19
VIO_22

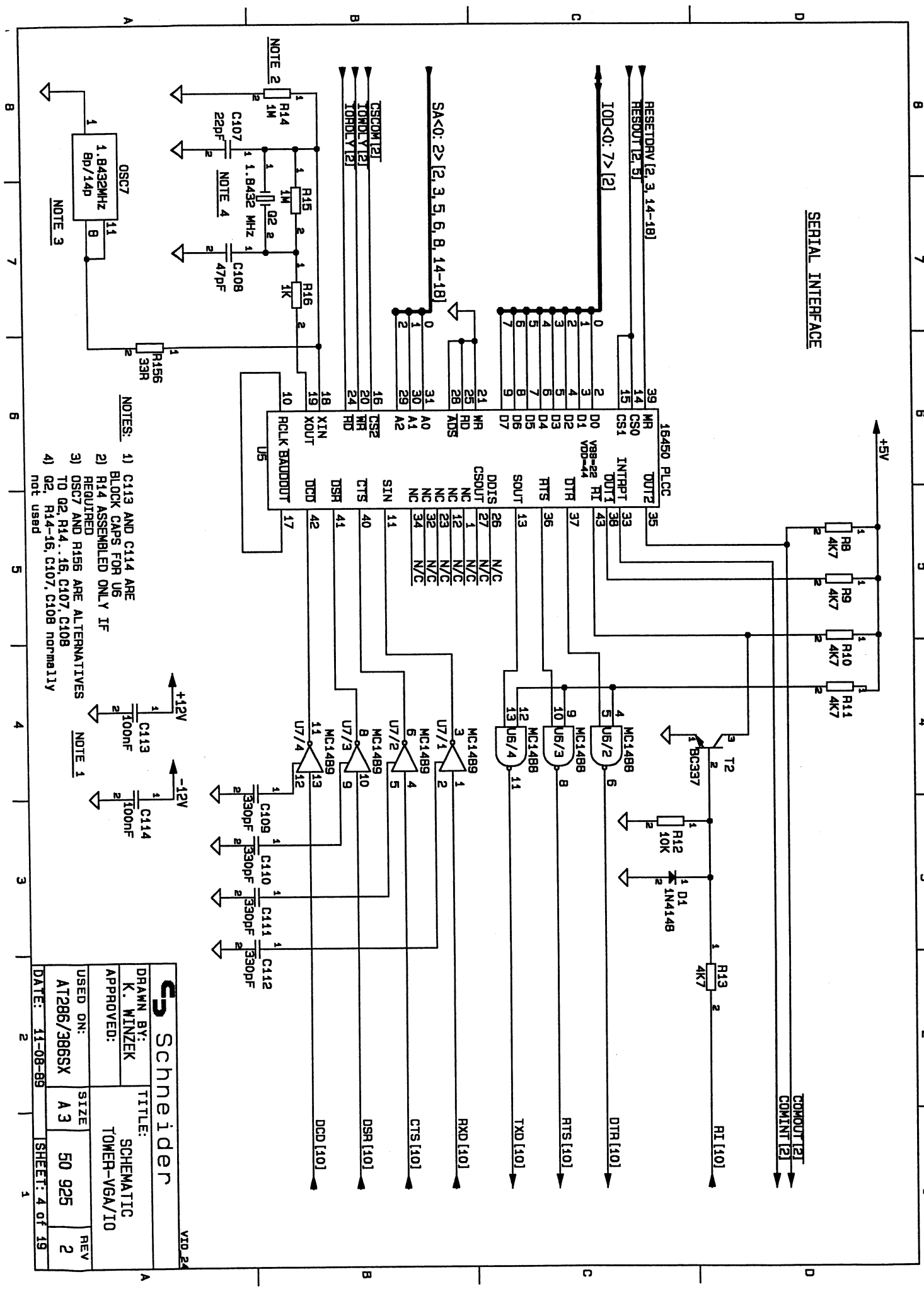
FLOPPY INTERFACE

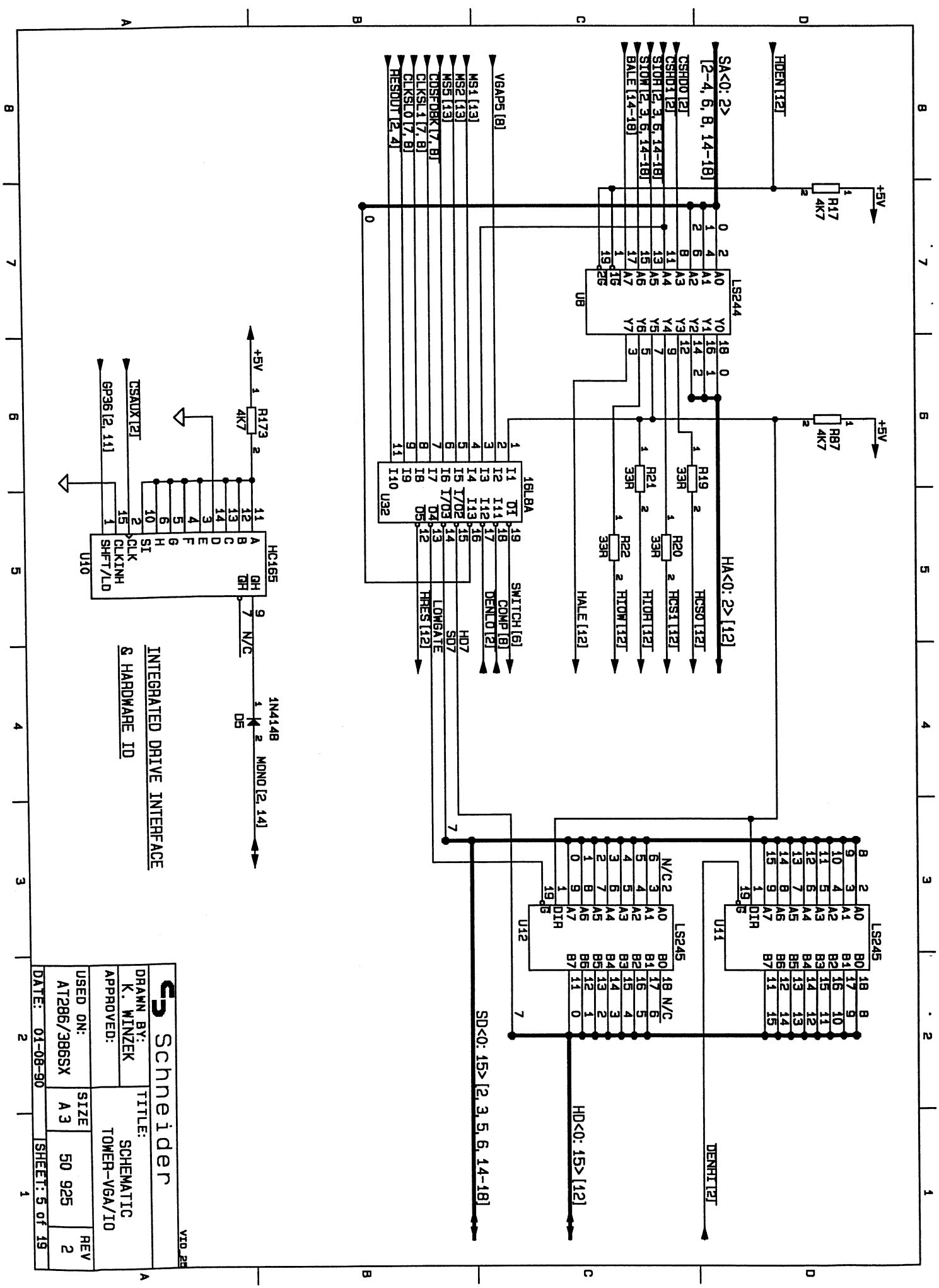


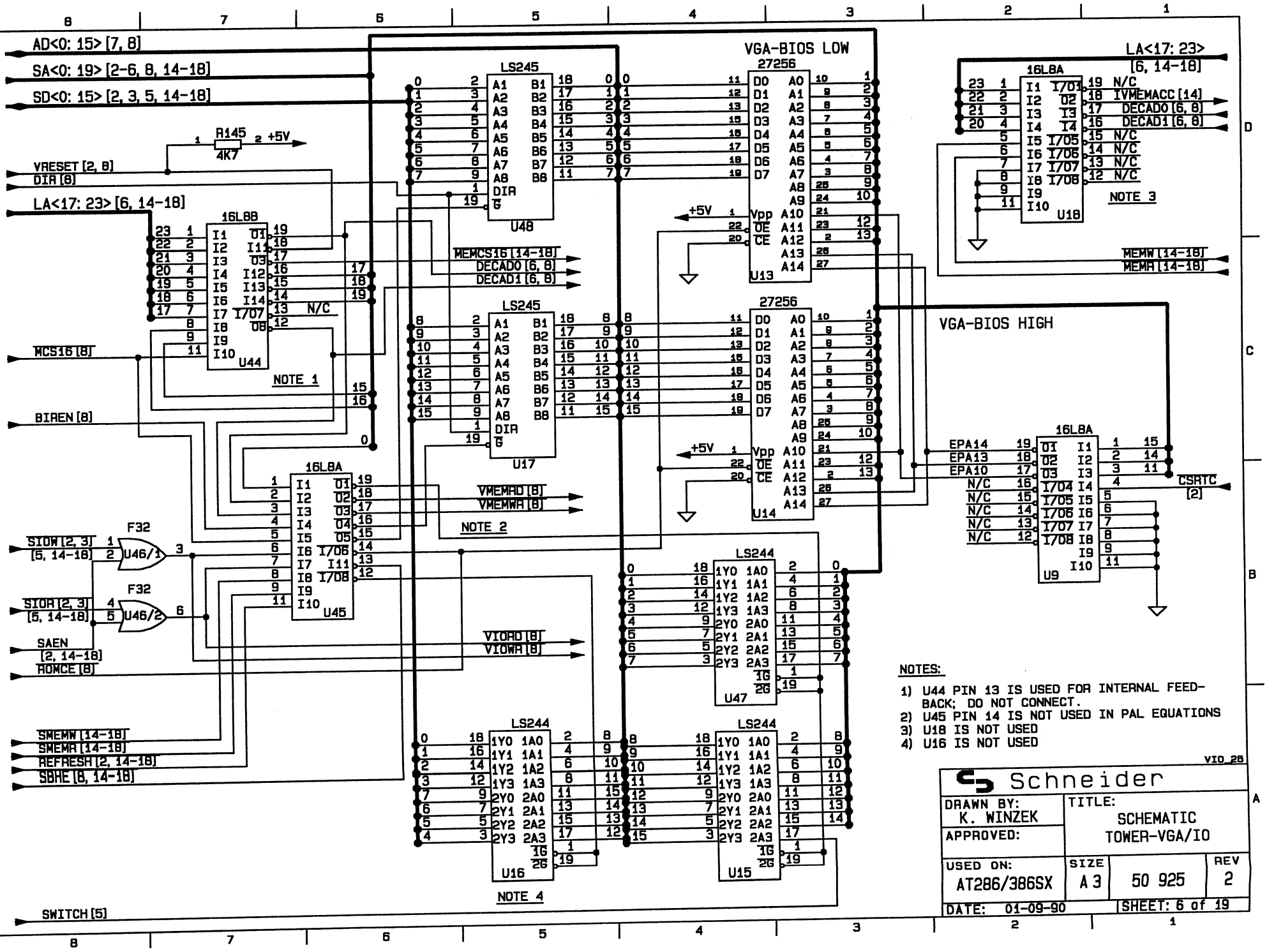
NOTES:
1) JS2 SELECTS WRITE PRECOMP. VAL.:
   JS2 OPEN : 125 ns
   JS2 CLOSED: 187 ns
2) JS3 SELECTS 2 SPEED SPINDLE DRIVE IF CLOSED
3) C103 IS BLOCK CAP FOR OSC1
4) C104 IS BLOCK CAP FOR OSC2
5) EITHER OSC2, R7 OR Q1, C105, C106 ARE INSERTED
6) R7 MAY BE 0 OHM (BRIDGE)
7) OSC2, R7 normally not used

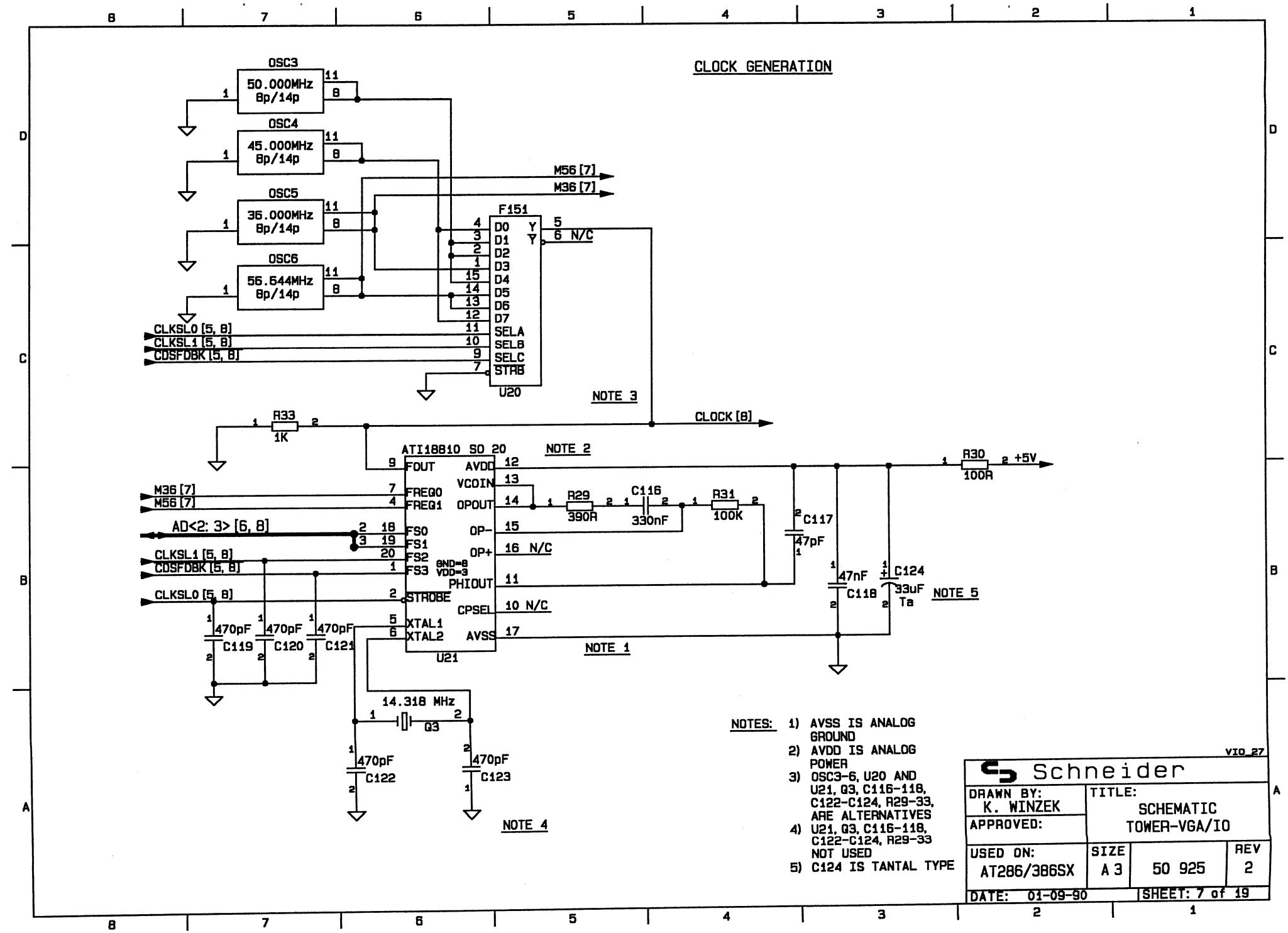
VID_23

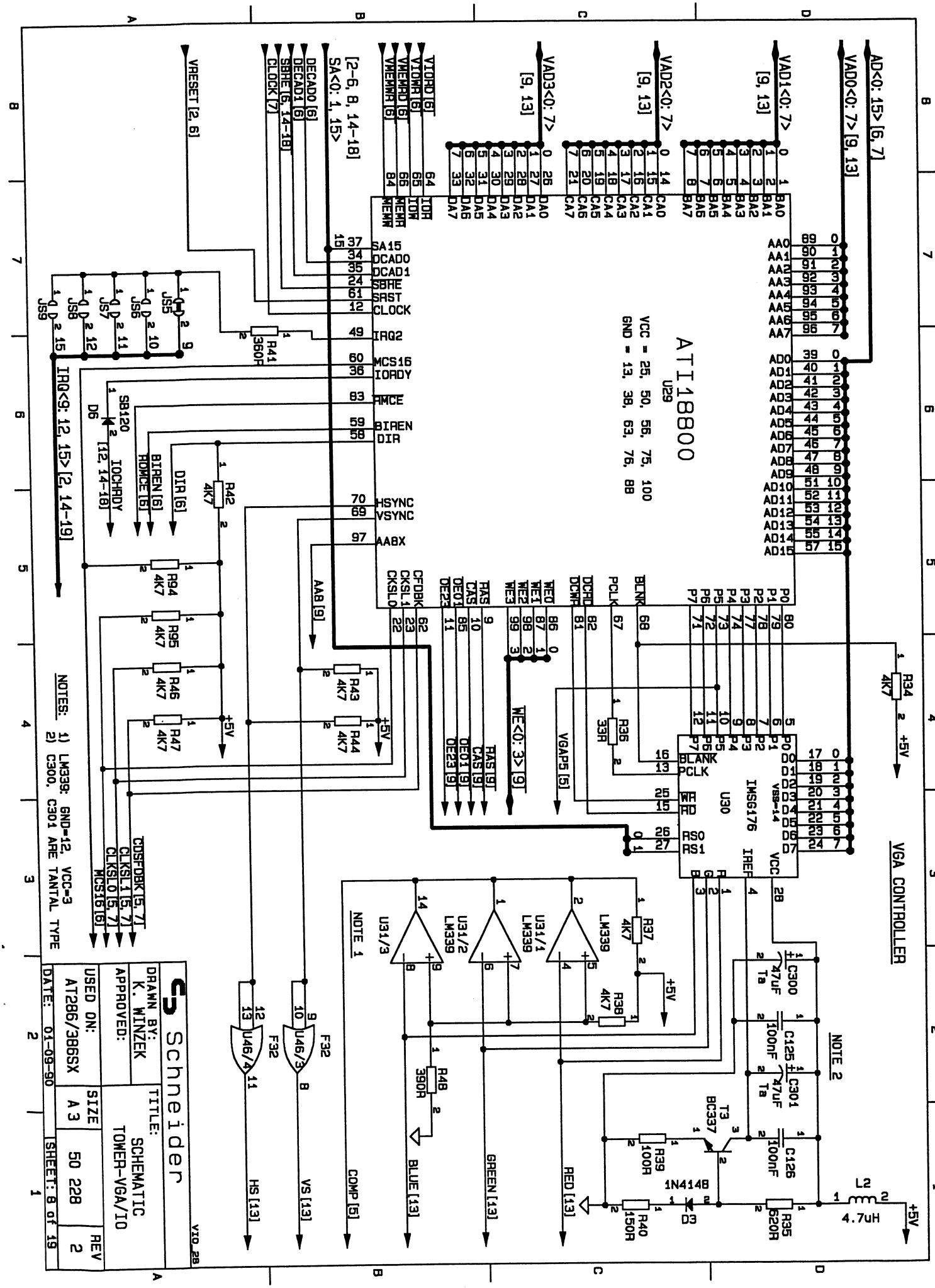
Schneider			
DRAWN BY: K. WINZEK	TITLE: SCHEMATIC TOWER-VGA/IO		
APPROVED:			
USED ON: AT286/386SX	SIZE A 3	50 925	REV 2
DATE: 01-05-90	SHEET: 3 of 19		

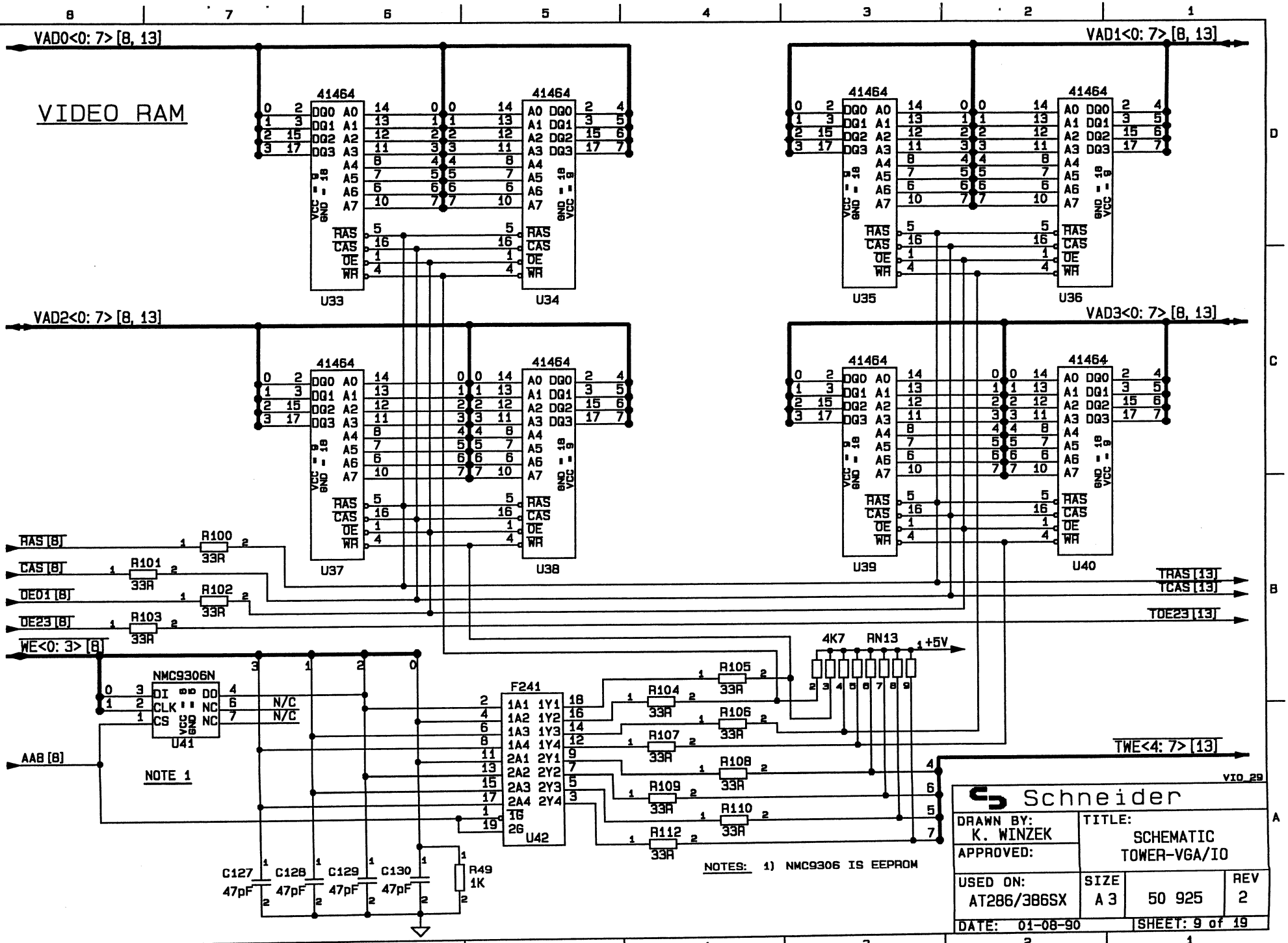

SERIAL INTERFACE
RESETDRV [2, 3, 14-18]
RESOUT [2, 5]
IOD<0: 7> [2]
SA<0: 2> [2, 3, 5, 6, 8, 14-18]
CSCOM [2]
IOWDLY [2]
IORDLY [2]
16450 PLCC
U5
U6
U7
+5V
+12V
-12V
R8 4K7
R9 4K7
R10 4K7
R11 4K7
R12 10K
R13 4K7
R14 1M
R15 1M
R16 1K
R156 33R
C107 22pF
C108 47pF
C109 330pF
C110 330pF
C111 330pF
C112 330pF
C113 100nF
C114 100nF
Q2 1.8432 MHz
OSC7 1.8432MHz 8p/14p
T2 BC337
D1 1N4148
MC1488
MC1489
NOTE 1
NOTE 2
NOTE 3
NOTE 4
NOTES:
1) C113 AND C114 ARE BLOCK CAPS FOR U6
2) R14 ASSEMBLED ONLY IF REQUIRED
3) OSC7 AND R156 ARE ALTERNATIVES TO Q2, R14..16, C107, C108
4) Q2, R14-16, C107, C108 normally not used
COMOUT [2]
COMINT [2]
RI [10]
DTR [10]
RTS [10]
TXD [10]
RXD [10]
CTS [10]
DSR [10]
DCD [10]
Schneider
DRAWN BY: K. WINZEK
APPROVED:
TITLE: SCHEMATIC TOWER-VGA/IO
USED ON: AT286/386SX
SIZE A 3
50 925
REV 2
DATE: 11-08-89
SHEET: 4 of 19

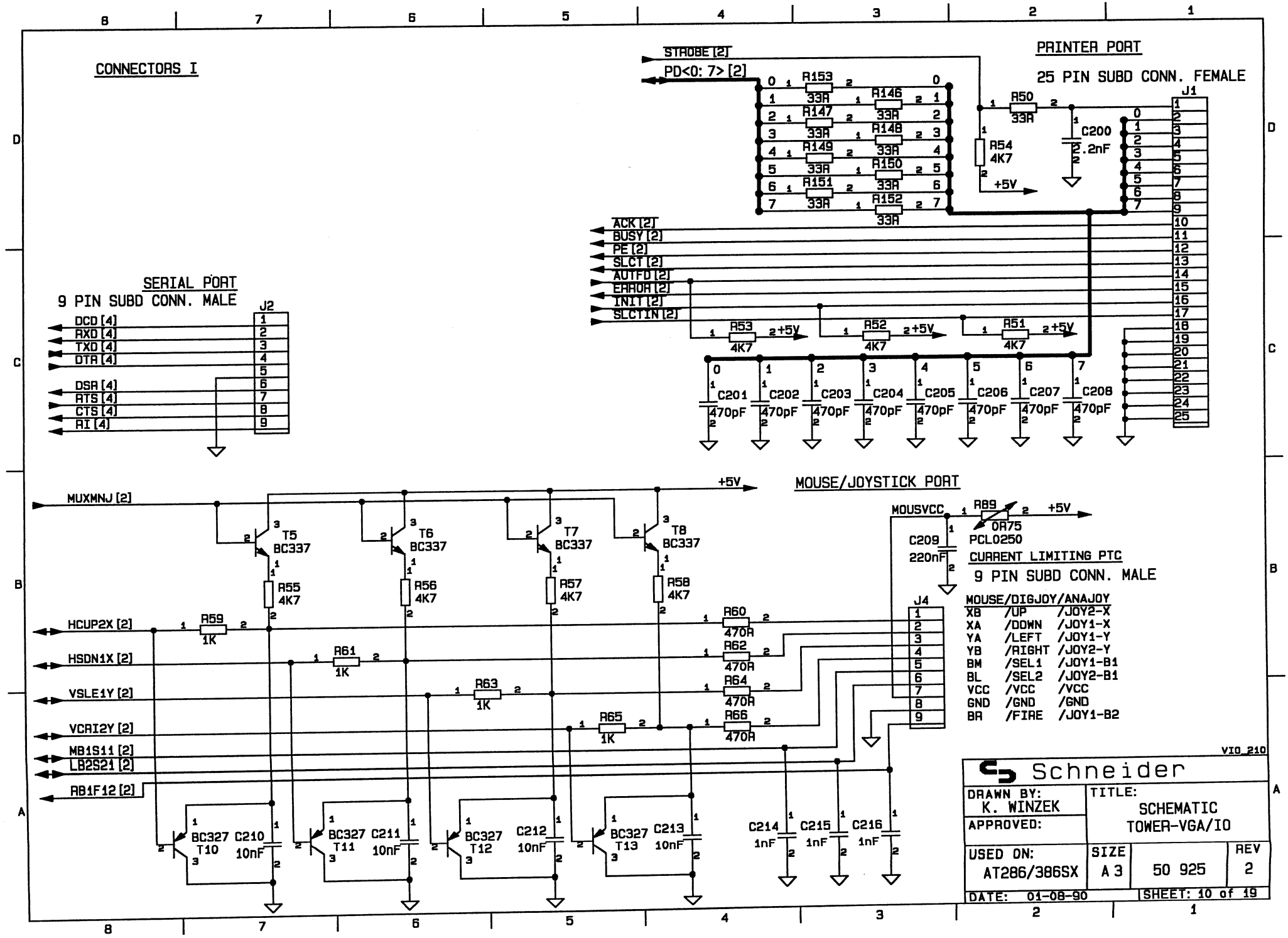

INTEGRATED DRIVE INTERFACE
& HARDWARE ID
Schneider
DRAWN BY: K. WINZEK
APPROVED:
TITLE: SCHEMATIC TOWER-VGA/IO
USED ON: AT286/386SX
SIZE A 3
50 925
REV 2
DATE: 01-08-90
SHEET: 5 of 19
VIO 25


AD<0: 15> [7, 8]
SA<0: 19> [2-6, 8, 14-18]
SD<0: 15> [2, 3, 5, 14-18]
R145
4K7
+5V
VRESET [2, 8]
DIR [8]
LA<17: 23> [6, 14-18]
16L8B
U44
NOTE 1
MCS16 [8]
BIAEN [8]
16L8A
U45
F32
U46/1
U46/2
SIOW [2, 3] [5, 14-18]
SIOR [2, 3] [5, 14-18]
SAEN [2, 14-18]
ROMCE [8]
SMEMW [14-18]
SMEMR [14-18]
REFRESH [2, 14-18]
SBHE [8, 14-18]
SWITCH [5]
LS245
U48
U17
MEMCS16 [14-18]
DECADO [6, 8]
DECAD1 [6, 8]
VMEMRD [8]
VMEMWR [8]
NOTE 2
VIORD [8]
VIOWR [8]
LS244
U16
U47
U15
NOTE 4
VGA-BIOS LOW
27256
U13
U14
VGA-BIOS HIGH
U18
U9
NOTE 3
MEMW [14-18]
MEMR [14-18]
EPA14
EPA13
EPA10
CSRTC [2]
NOTES:
1) U44 PIN 13 IS USED FOR INTERNAL FEED-BACK; DO NOT CONNECT.
2) U45 PIN 14 IS NOT USED IN PAL EQUATIONS
3) U18 IS NOT USED
4) U16 IS NOT USED
Schneider
DRAWN BY: K. WINZEK
APPROVED:
TITLE: SCHEMATIC TOWER-VGA/IO
USED ON: AT286/386SX
SIZE A 3
50 925
REV 2
DATE: 01-09-90
SHEET: 6 of 19
VIO_2B

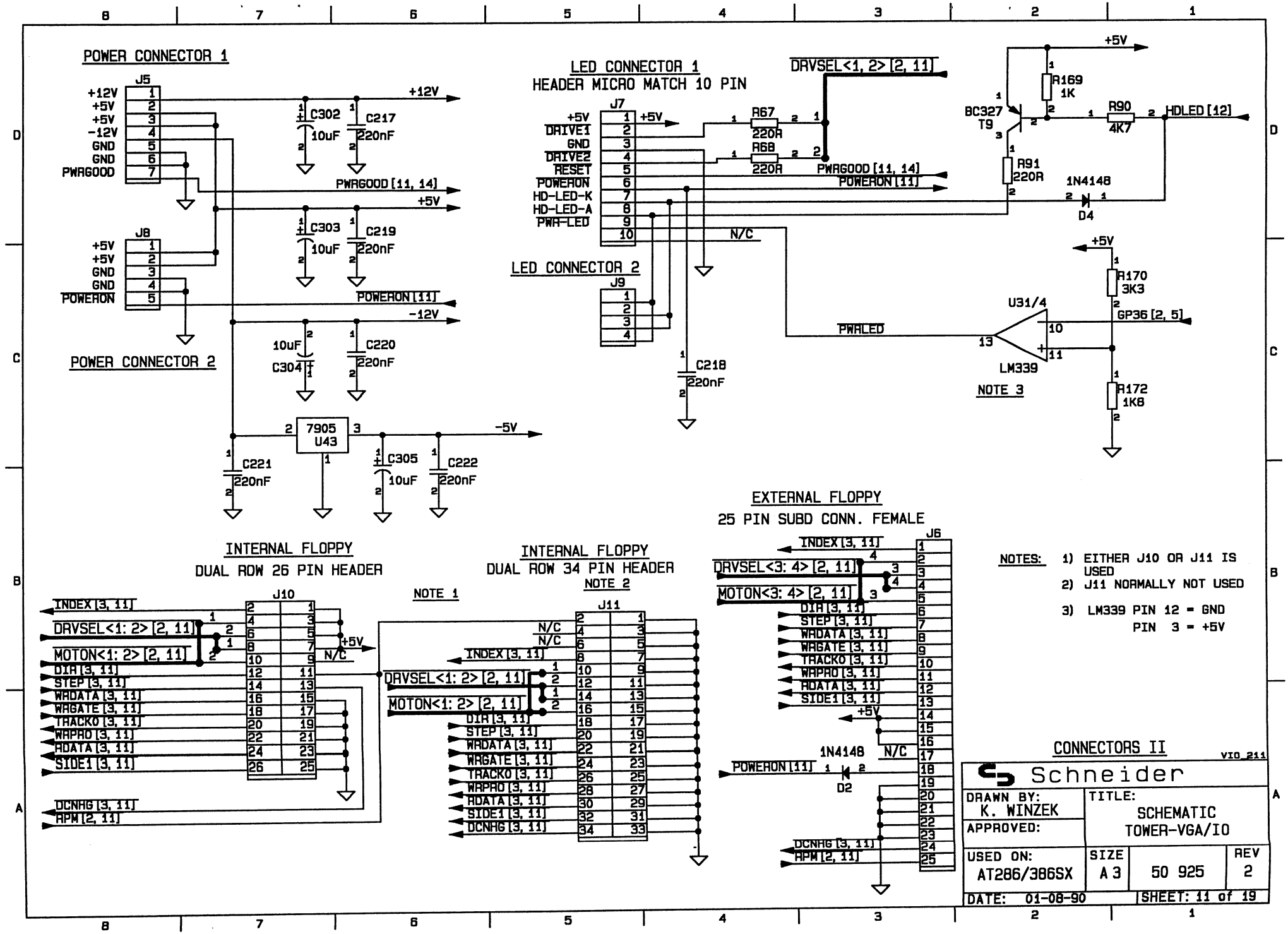

CLOCK GENERATION
OSC3
50.000MHz
8p/14p
OSC4
45.000MHz
8p/14p
OSC5
36.000MHz
8p/14p
OSC6
56.644MHz
8p/14p
M56 [7]
M36 [7]
F151
D0
D1
D2
D3
D4
D5
D6
D7
SELA
SELB
SELC
STRB
Y
Y
N/C
U20
NOTE 3
CLKSL0 [5, 8]
CLKSL1 [5, 8]
CDSFDBK [5, 8]
R33
1K
CLOCK [8]
ATI18810 SO 20
NOTE 2
FOUT
FREQ0
FREQ1
FS0
FS1
FS2
FS3
STROBE
XTAL1
XTAL2
AVDD
VCOIN
OPOUT
OP-
OP+
PHIOUT
CPSEL
AVSS
GND=8
VDD=3
R30
100R
+5V
R29
390R
C116
330nF
R31
100K
C117
47pF
C118
47nF
C124
33uF
Ta
NOTE 5
NOTE 1
AD<2: 3> [6, 8]
C119
470pF
C120
470pF
C121
470pF
U21
14.318 MHz
Q3
C122
470pF
C123
470pF
NOTE 4
NOTES: 1) AVSS IS ANALOG GROUND
2) AVDD IS ANALOG POWER
3) OSC3-6, U20 AND U21, Q3, C116-118, C122-C124, R29-33, ARE ALTERNATIVES
4) U21, Q3, C116-118, C122-C124, R29-33 NOT USED
5) C124 IS TANTAL TYPE
VIO_27
Schneider
DRAWN BY: K. WINZEK
APPROVED:
TITLE: SCHEMATIC TOWER-VGA/IO
USED ON: AT286/386SX
SIZE A 3
50 925
REV 2
DATE: 01-09-90
SHEET: 7 of 19


VGA CONTROLLER
ATI18800
U29
VCC = 25, 50, 56, 75, 100
GND = 13, 38, 63, 76, 88
IMS6176
U30
VSS=14
VCC
IREF
BLANK
PCLK
RD
WR
RS0
RS1
AD<0:15> [6,7]
VAD0<0:7> [9,13]
VAD1<0:7> [9,13]
VAD2<0:7> [9,13]
VAD3<0:7> [9,13]
[2-6,8,14-18] SA<0:1,15>
VRESET [2,6]
IRQ<9,12,15> [2,14-19]
SA15
DCAD0
DCAD1
SBHE
SRST
CLOCK
IRQ2
MCS16
IORDY
AMCE
BIREN
DIR
HSYNC
VSYNC
AA8X
CFDBK
CKSL1
CKSL0
RAS
CAS
OE01
OE23
WE0
WE1
WE2
WE3
DCMD
DCMR
BLNK
PCLK
P0
P1
P2
P3
P4
P5
P6
P7
AA0
AA1
AA2
AA3
AA4
AA5
AA6
AA7
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
D0
D1
D2
D3
D4
D5
D6
D7
VGAP5 [5]
WE<0:3> [9]
RAS [9]
CAS [9]
OE01 [9]
OE23 [9]
AA8 [9]
R34 4K7
R36 33R
R37 4K7
R38 4K7
R39 100R
R40 150R
R41 360R
R42 4K7
R43 4K7
R44 4K7
R46 4K7
R47 4K7
R48 390R
R94 4K7
R95 4K7
C300 47uF Ta
C125 100nF
C301 47uF Ta
C126 100nF
L2 4.7uH
D3 1N4148
T3 BC337
U31/1 LM339
U31/2 LM339
U31/3 LM339
U46/3
U46/4
F32
F32
NOTE 1
NOTE 2
SB120 D6
IOCHRDY [12,14-18]
BIREN [6]
AMCE [6]
DIR [6]
JS5
JS6
JS7
JS8
JS9
+5V
COMP [5]
RED [13]
GREEN [13]
BLUE [13]
VS [13]
HS [13]
CFDBK [5,7]
CLKSL1 [5,7]
CLKSL0 [5,7]
MCS16 [6]
NOTES: 1) LM339: GND=12, VCC=3
2) C300, C301 ARE TANTAL TYPE
Schneider
VIO_28
DRAWN BY: K. WINZEK
APPROVED:
TITLE: SCHEMATIC TOWER-VGA/IO
USED ON: AT286/386SX
SIZE A 3
REV 2
DATE: 01-09-90
SHEET: 8 of 19
50 228


VIDEO RAM
VAD0<0: 7> [8, 13]
VAD1<0: 7> [8, 13]
VAD2<0: 7> [8, 13]
VAD3<0: 7> [8, 13]
41464
U33
U34
U35
U36
U37
U38
U39
U40
RAS [8]
CAS [8]
OE01 [8]
OE23 [8]
WE<0: 3> [8]
AA8 [8]
R100 33R
R101 33R
R102 33R
R103 33R
NMC9306N
U41
NOTE 1
N/C
F241
U42
4K7 RN13
+5V
R104 33R
R105 33R
R106 33R
R107 33R
R108 33R
R109 33R
R110 33R
R112 33R
C127 47pF
C128 47pF
C129 47pF
C130 47pF
R49 1K
TRAS [13]
TCAS [13]
TOE23 [13]
TWE<4: 7> [13]
NOTES: 1) NMC9306 IS EEPROM
VIO 29
Schneider
DRAWN BY: K. WINZEK
APPROVED:
TITLE: SCHEMATIC TOWER-VGA/IO
USED ON: AT286/386SX
SIZE A 3
50 925
REV 2
DATE: 01-08-90
SHEET: 9 of 19

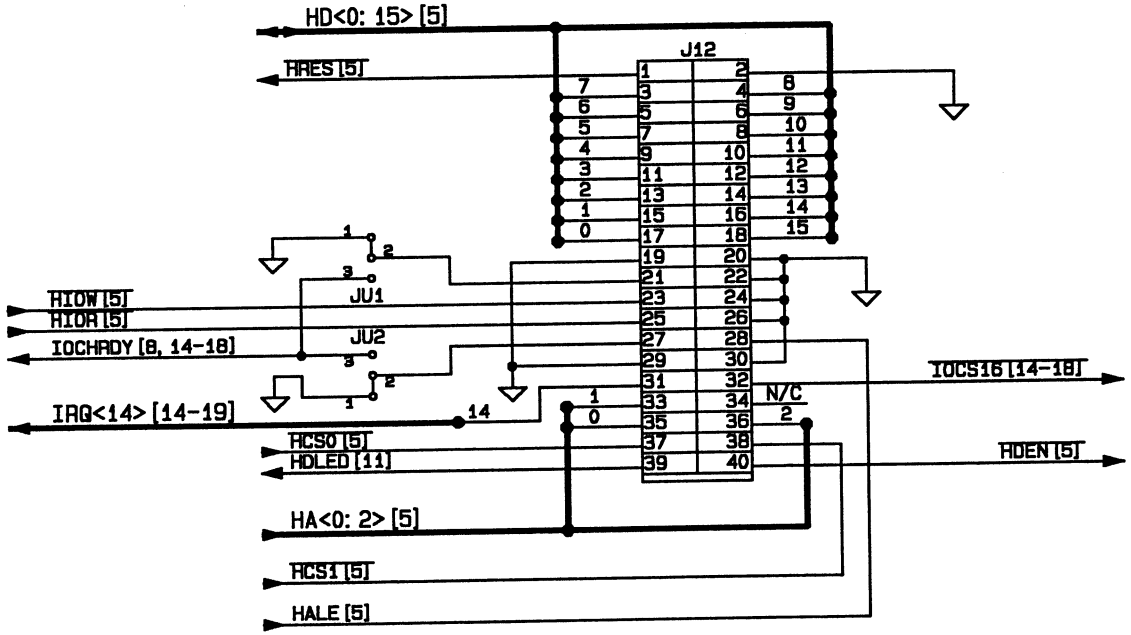

CONNECTORS I
PRINTER PORT
25 PIN SUBD CONN. FEMALE
J1
STROBE [2]
PD<0: 7> [2]
R153
R146
R147
R148
R149
R150
R151
R152
33R
R50
33R
C200
2.2nF
R54
4K7
+5V
ACK [2]
BUSY [2]
PE [2]
SLCT [2]
AUTFD [2]
ERROR [2]
INIT [2]
SLCTIN [2]
R53
R52
R51
4K7
C201
C202
C203
C204
C205
C206
C207
C208
470pF
SERIAL PORT
9 PIN SUBD CONN. MALE
J2
DCD [4]
RXD [4]
TXD [4]
DTR [4]
DSR [4]
RTS [4]
CTS [4]
RI [4]
MOUSE/JOYSTICK PORT
MUXMNJ [2]
T5
T6
T7
T8
BC337
R55
R56
R57
R58
4K7
HCUP2X [2]
HSDN1X [2]
VSLE1Y [2]
VCRI2Y [2]
MB1S11 [2]
LB2S21 [2]
RB1F12 [2]
R59
R61
R63
R65
1K
R60
R62
R64
R66
470R
MOUSVCC
R89
0R75
PCL0250
CURRENT LIMITING PTC
C209
220nF
9 PIN SUBD CONN. MALE
J4
MOUSE/DIGJOY/ANAJOY
XB /UP /JOY2-X
XA /DOWN /JOY1-X
YA /LEFT /JOY1-Y
YB /RIGHT /JOY2-Y
BM /SEL1 /JOY1-B1
BL /SEL2 /JOY2-B1
VCC /VCC /VCC
GND /GND /GND
BR /FIRE /JOY1-B2
T10
T11
T12
T13
BC327
C210
C211
C212
C213
10nF
C214
C215
C216
1nF
VIO 210
Schneider
DRAWN BY: K. WINZEK
APPROVED:
TITLE: SCHEMATIC TOWER-VGA/IO
USED ON: AT286/386SX
SIZE A3
50 925
REV 2
DATE: 01-08-90
SHEET: 10 of 19

21


POWER CONNECTOR 1
J5
+12V 1
+5V 2
+5V 3
-12V 4
GND 5
GND 6
PWRGOOD 7
C302 10uF
C217 220nF
+12V
PWRGOOD [11, 14]
+5V
C303 10uF
C219 220nF
J8
+5V 1
+5V 2
GND 3
GND 4
POWERON 5
POWERON [11]
-12V
10uF C304
C220 220nF
POWER CONNECTOR 2
7905 U43
-5V
C221 220nF
C305 10uF
C222 220nF
LED CONNECTOR 1
HEADER MICRO MATCH 10 PIN
J7
+5V 1
DRIVE1 2
GND 3
DRIVE2 4
RESET 5
POWERON 6
HD-LED-K 7
HD-LED-A 8
PWR-LED 9
10
+5V
DRVSEL<1, 2> [2, 11]
R67 220R
R68 220R
PWRGOOD [11, 14]
POWERON [11]
N/C
LED CONNECTOR 2
J9
C218 220nF
PWRLED
+5V
R169 1K
BC327 T9
R90 4K7
HDLED [12]
R91 220R
1N4148
D4
+5V
R170 3K3
U31/4
GP36 [2, 5]
LM339
NOTE 3
R172 1K8
INTERNAL FLOPPY
DUAL ROW 26 PIN HEADER
J10
INDEX [3, 11]
DRVSEL<1: 2> [2, 11]
MOTON<1: 2> [2, 11]
DIR [3, 11]
STEP [3, 11]
WRDATA [3, 11]
WRGATE [3, 11]
TRACK0 [3, 11]
WRPRO [3, 11]
RDATA [3, 11]
SIDE1 [3, 11]
+5V
N/C
DCNHG [3, 11]
RPM [2, 11]
NOTE 1
INTERNAL FLOPPY
DUAL ROW 34 PIN HEADER
NOTE 2
J11
N/C
N/C
INDEX [3, 11]
DRVSEL<1: 2> [2, 11]
MOTON<1: 2> [2, 11]
DIR [3, 11]
STEP [3, 11]
WRDATA [3, 11]
WRGATE [3, 11]
TRACK0 [3, 11]
WRPRO [3, 11]
RDATA [3, 11]
SIDE1 [3, 11]
DCNHG [3, 11]
EXTERNAL FLOPPY
25 PIN SUBD CONN. FEMALE
J6
INDEX [3, 11]
DRVSEL<3: 4> [2, 11]
MOTON<3: 4> [2, 11]
DIR [3, 11]
STEP [3, 11]
WRDATA [3, 11]
WRGATE [3, 11]
TRACK0 [3, 11]
WRPRO [3, 11]
RDATA [3, 11]
SIDE1 [3, 11]
+5V
1N4148
N/C
POWERON [11]
D2
DCNHG [3, 11]
RPM [2, 11]
NOTES: 1) EITHER J10 OR J11 IS USED
2) J11 NORMALLY NOT USED
3) LM339 PIN 12 = GND
PIN 3 = +5V
CONNECTORS II
VIO_211
Schneider
DRAWN BY: K. WINZEK
APPROVED:
TITLE: SCHEMATIC TOWER-VGA/IO
USED ON: AT286/386SX
SIZE A 3
50 925
REV 2
DATE: 01-08-90
SHEET: 11 of 19

AT INTEGRATED DRIVE CONNECTOR

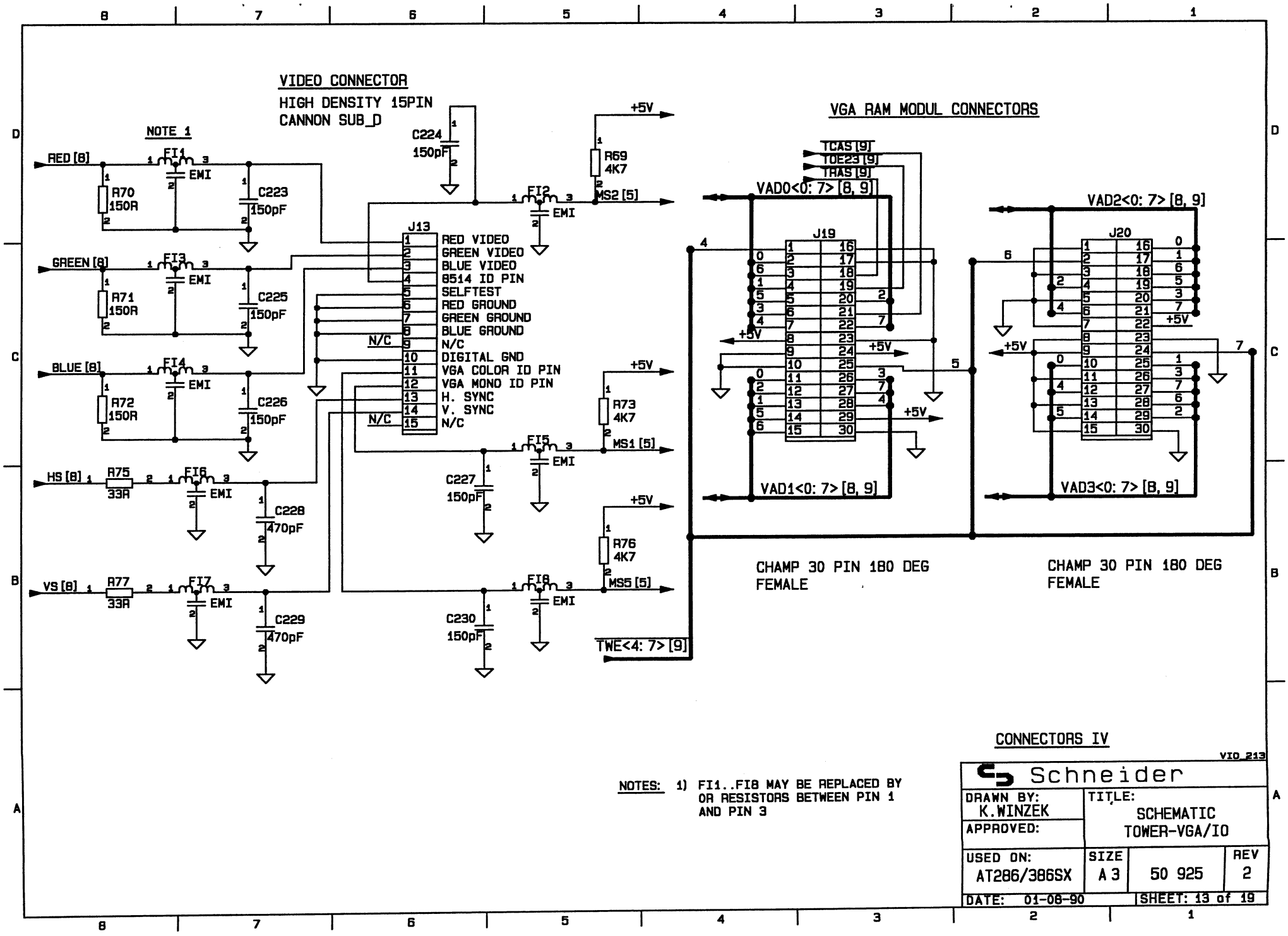
40 PIN HEADER DUAL ROW



CONNECTORS III

VIO_212

Schneider			
DRAWN BY: K. WINZEK	TITLE: SCHEMATIC TOWER-VGA/IO		
APPROVED:			
USED ON: AT286/386SX	SIZE A 3	50 925	REV 2
DATE: 01-05-90	SHEET: 12 of 19		

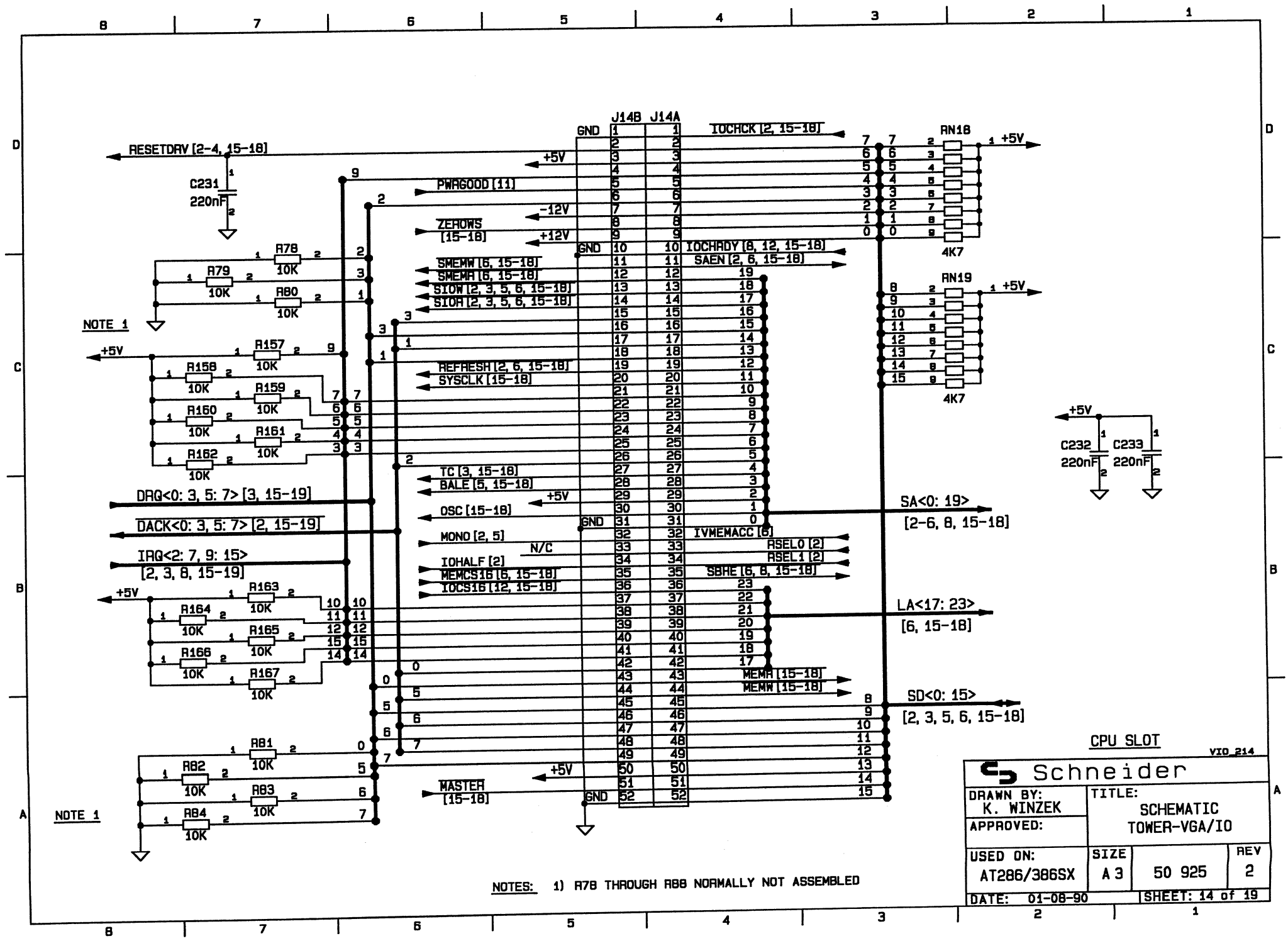


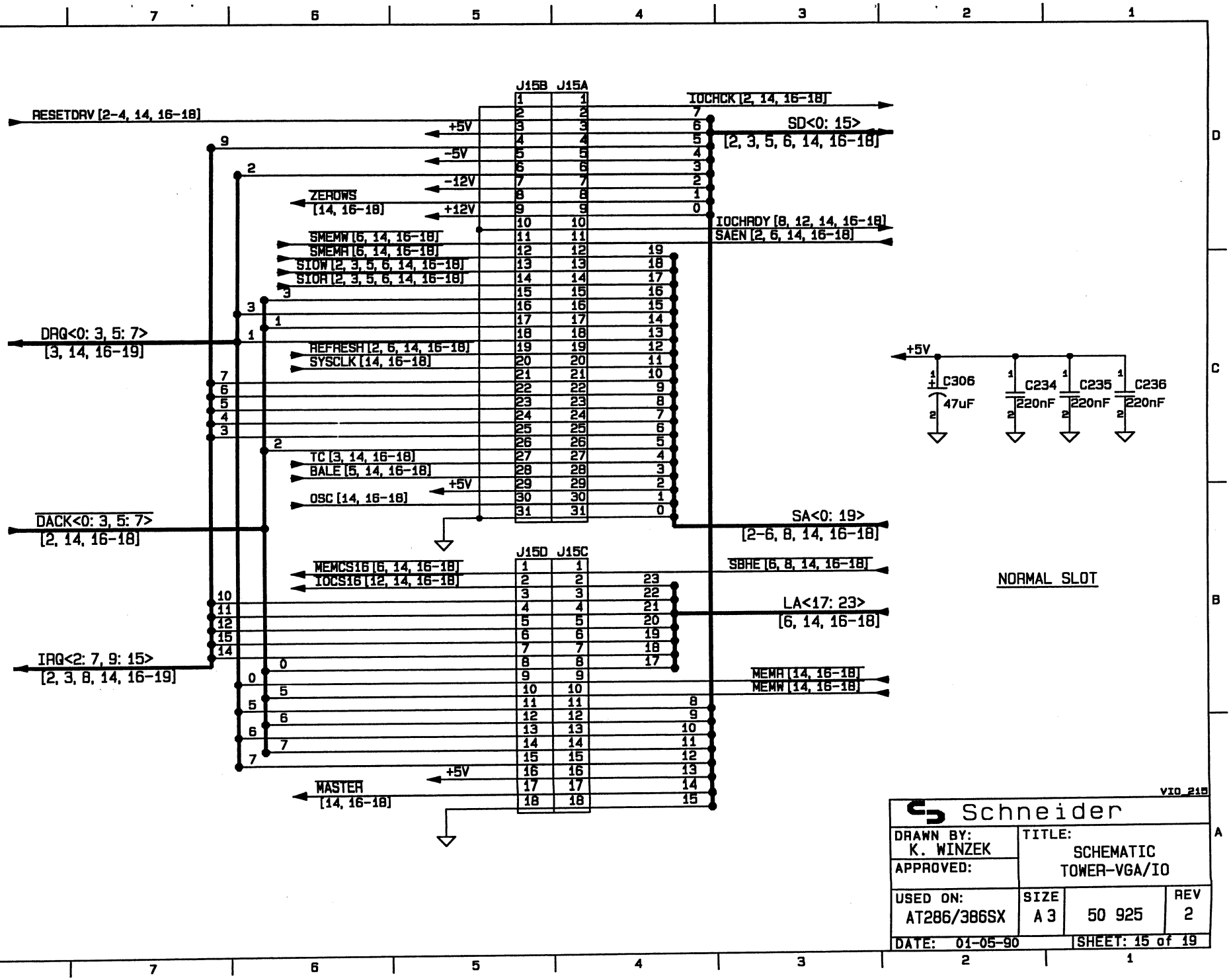
NOTES: 1) FI1..FI8 MAY BE REPLACED BY OR RESISTORS BETWEEN PIN 1 AND PIN 3

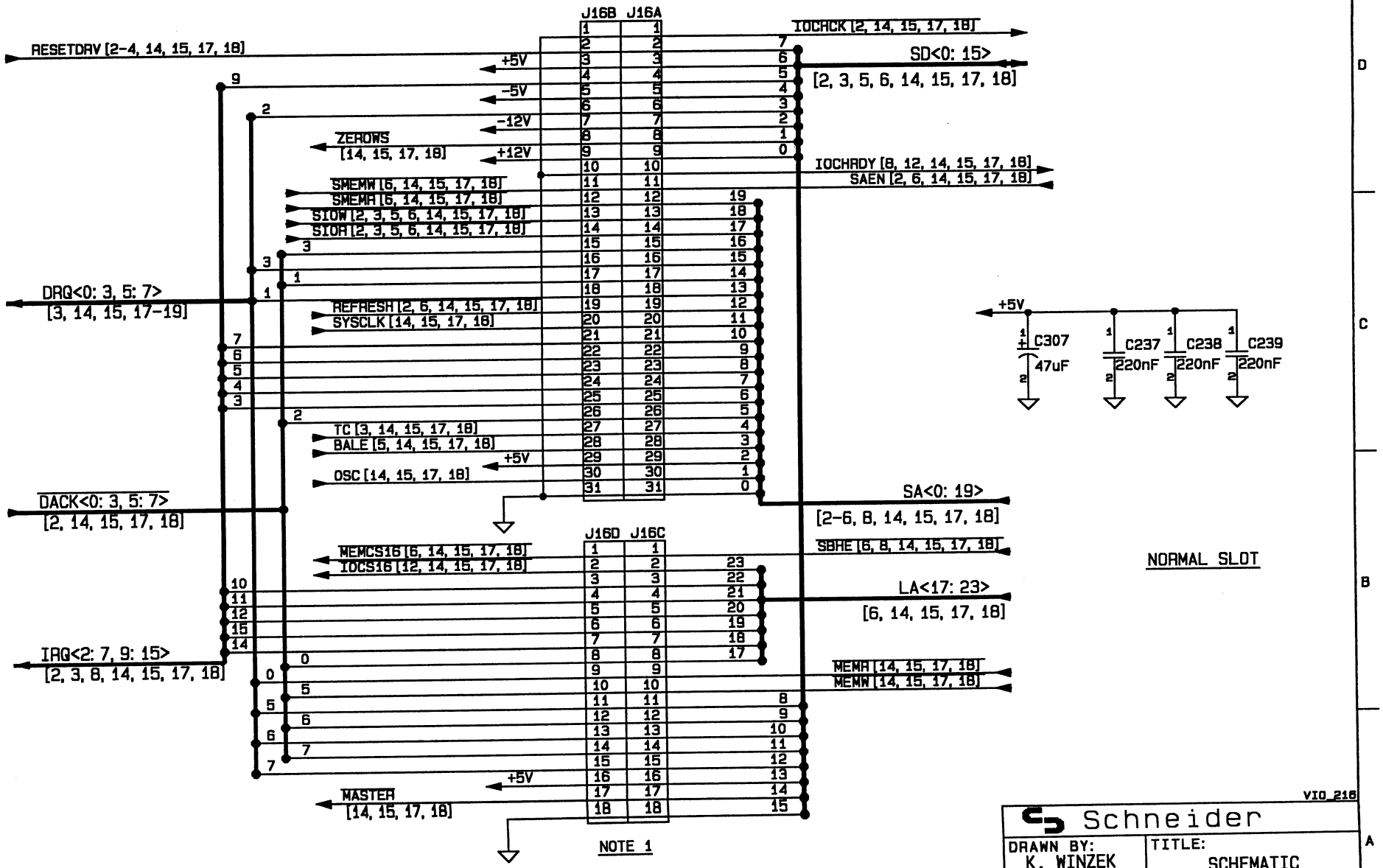
CONNECTORS IV

VIO_213

Schneider			
DRAWN BY: K.WINZEK	TITLE: SCHEMATIC TOWER-VGA/IO		
APPROVED:			
USED ON: AT286/386SX	SIZE A 3	50 925	REV 2
DATE: 01-08-90	SHEET: 13 of 19		

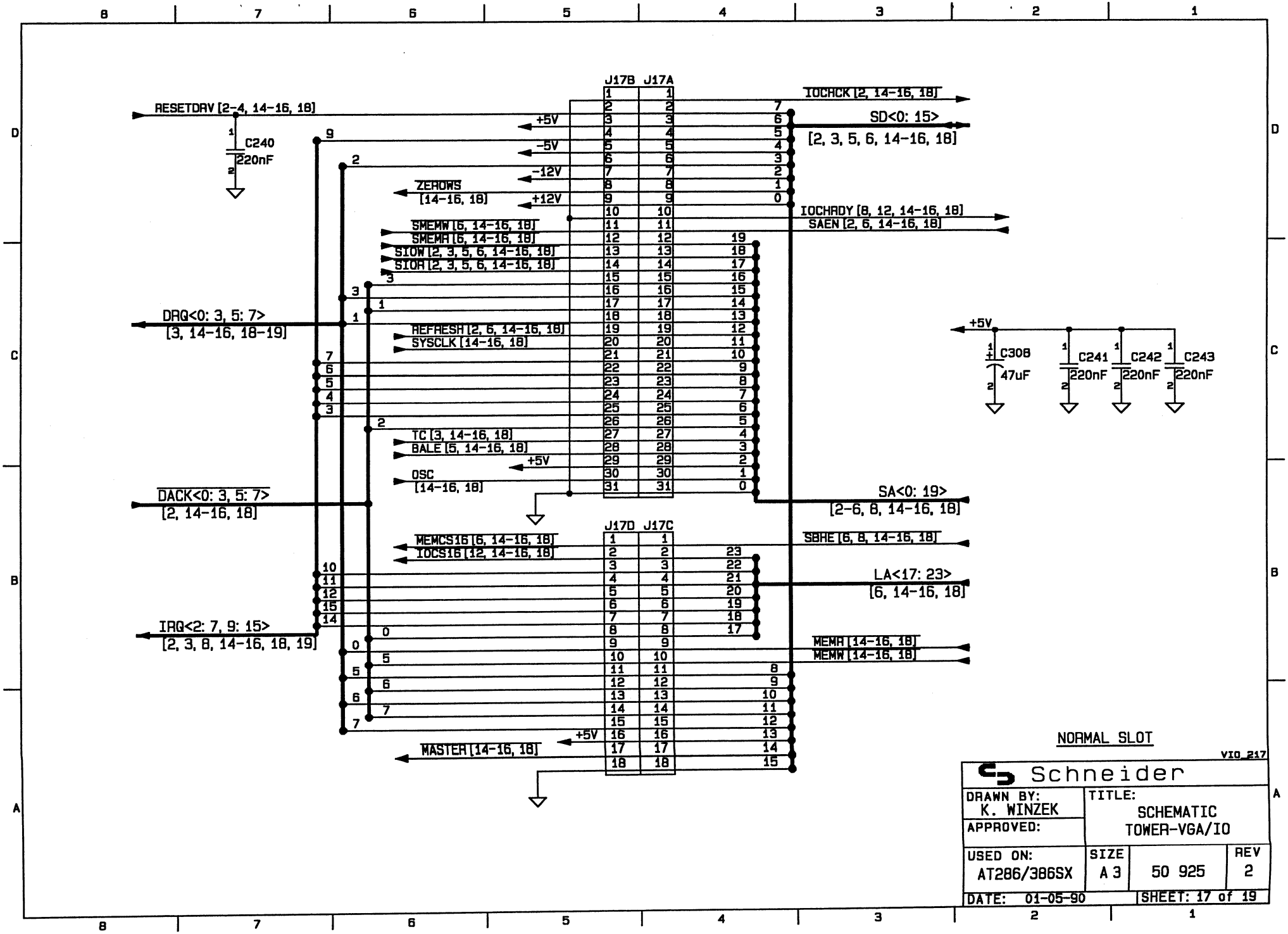

J14B J14A
RESETDRV [2-4, 15-18]
C231
220nF
PWRGOOD [11]
ZEROWS [15-18]
+5V
-12V
+12V
GND
IOCHCK [2, 15-18]
IOCHRDY [8, 12, 15-18]
SAEN [2, 6, 15-18]
SMEMW [6, 15-18]
SMEMR [6, 15-18]
SIOW [2, 3, 5, 6, 15-18]
SIOR [2, 3, 5, 6, 15-18]
REFRESH [2, 6, 15-18]
SYSCLK [15-18]
TC [3, 15-18]
BALE [5, 15-18]
OSC [15-18]
MONO [2, 5]
IOHALF [2]
MEMCS16 [6, 15-18]
IOCS16 [12, 15-18]
IVMEMACC [6]
RSEL0 [2]
RSEL1 [2]
SBHE [6, 8, 15-18]
MEMR [15-18]
MEMW [15-18]
MASTER [15-18]
N/C
R78 10K
R79 10K
R80 10K
R157 10K
R158 10K
R159 10K
R160 10K
R161 10K
R162 10K
R163 10K
R164 10K
R165 10K
R166 10K
R167 10K
R81 10K
R82 10K
R83 10K
R84 10K
RN18 4K7
RN19 4K7
C232 220nF
C233 220nF
DRQ<0: 3, 5: 7> [3, 15-19]
DACK<0: 3, 5: 7> [2, 15-19]
IRQ<2: 7, 9: 15> [2, 3, 8, 15-19]
SA<0: 19> [2-6, 8, 15-18]
LA<17: 23> [6, 15-18]
SD<0: 15> [2, 3, 5, 6, 15-18]
NOTE 1
NOTE 1
NOTES: 1) R78 THROUGH R88 NORMALLY NOT ASSEMBLED
CPU SLOT
VIO_214
Schneider
DRAWN BY: K. WINZEK
APPROVED:
TITLE: SCHEMATIC TOWER-VGA/IO
USED ON: AT286/386SX
SIZE A3
50 925
REV 2
DATE: 01-08-90
SHEET: 14 of 19


J15B J15A
J15D J15C
RESETDRV [2-4, 14, 16-18]
+5V
-5V
-12V
+12V
ZEROWS [14, 16-18]
SMEMW [6, 14, 16-18]
SMEMR [6, 14, 16-18]
SIOW [2, 3, 5, 6, 14, 16-18]
SIOR [2, 3, 5, 6, 14, 16-18]
DRQ<0: 3, 5: 7> [3, 14, 16-19]
REFRESH [2, 6, 14, 16-18]
SYSCLK [14, 16-18]
TC [3, 14, 16-18]
BALE [5, 14, 16-18]
OSC [14, 16-18]
DACK<0: 3, 5: 7> [2, 14, 16-18]
MEMCS16 [6, 14, 16-18]
IOCS16 [12, 14, 16-18]
IRQ<2: 7, 9: 15> [2, 3, 8, 14, 16-19]
MASTER [14, 16-18]
IOCHCK [2, 14, 16-18]
SD<0: 15> [2, 3, 5, 6, 14, 16-18]
IOCHRDY [8, 12, 14, 16-18]
SAEN [2, 6, 14, 16-18]
SA<0: 19> [2-6, 8, 14, 16-18]
SBHE [6, 8, 14, 16-18]
LA<17: 23> [6, 14, 16-18]
MEMR [14, 16-18]
MEMW [14, 16-18]
+5V
C306 47uF
C234 220nF
C235 220nF
C236 220nF
NORMAL SLOT
VIO_215
Schneider
DRAWN BY: K. WINZEK
APPROVED:
TITLE: SCHEMATIC TOWER-VGA/IO
USED ON: AT286/386SX
SIZE A 3
50 925
REV 2
DATE: 01-05-90
SHEET: 15 of 19



NOTES: 1) CARD EDGE CONNECTOR J16C-D NOT ASSEMBLED

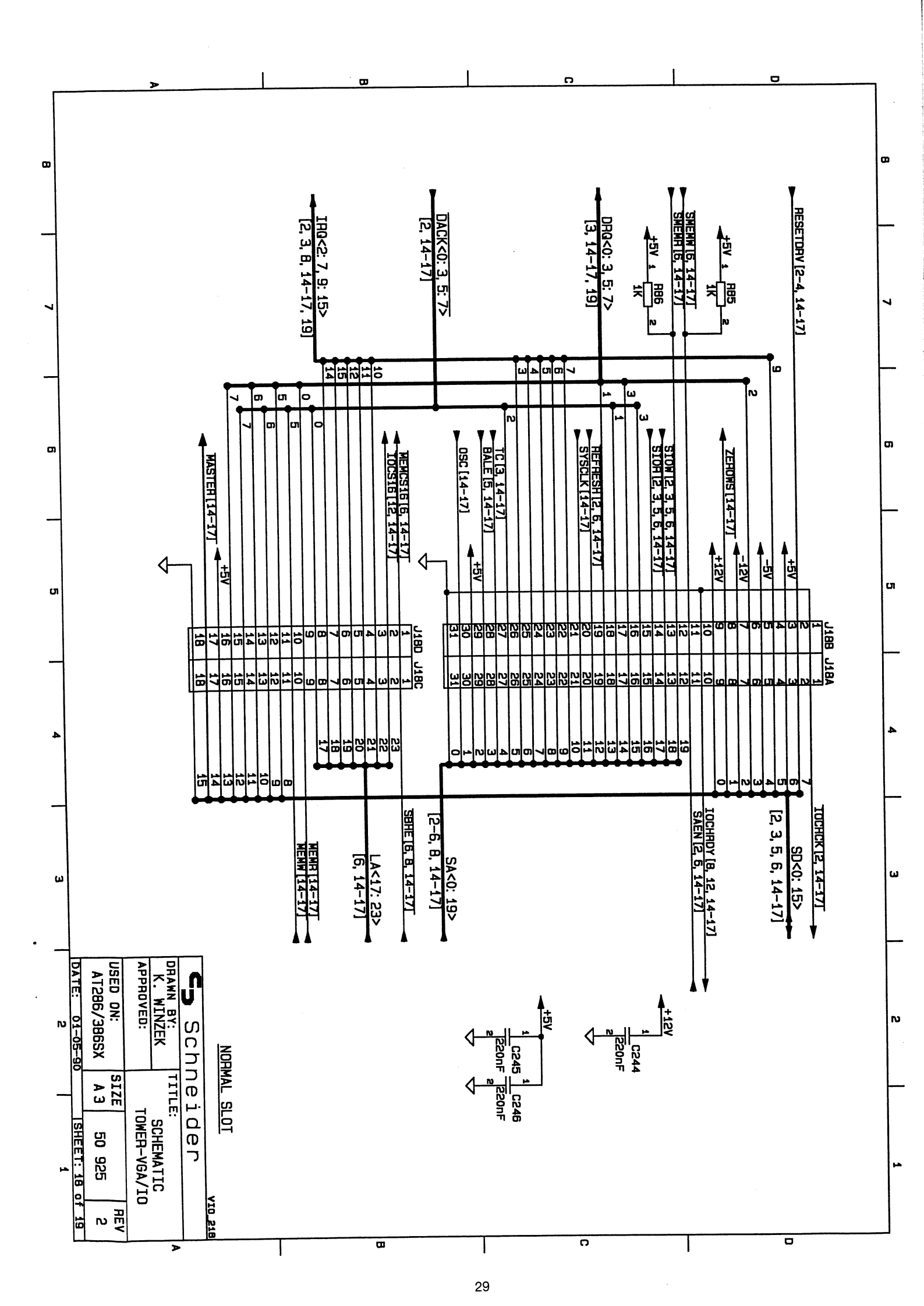
Schneider			VIO_218
DRAWN BY: K. WINZEK	TITLE: SCHEMATIC TOWER-VGA/IO		
APPROVED:			
USED ON: AT286/386SX	SIZE A 3	50 925	REV 2
DATE: 01-05-90	SHEET: 16 of 19		

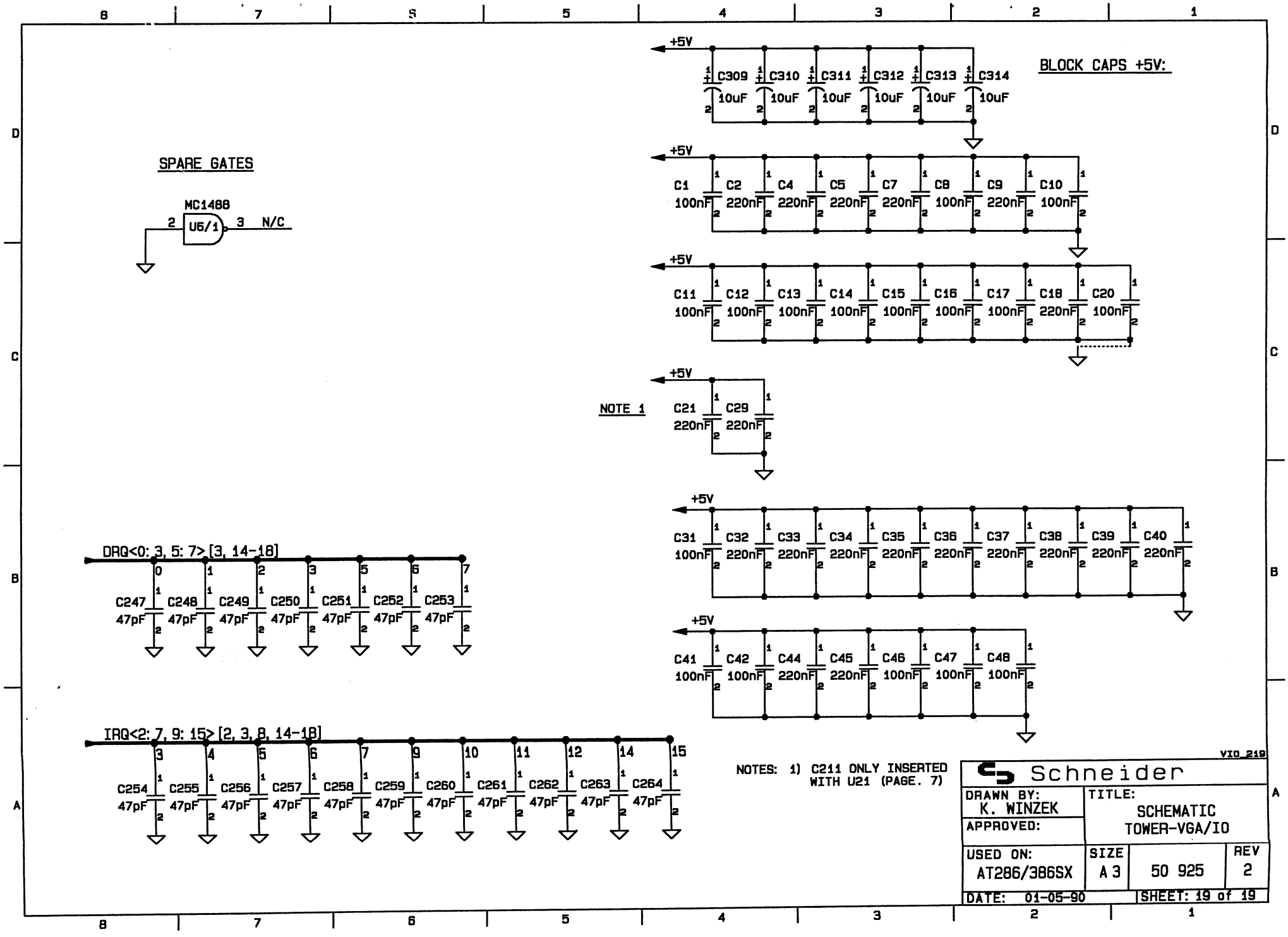


NORMAL SLOT

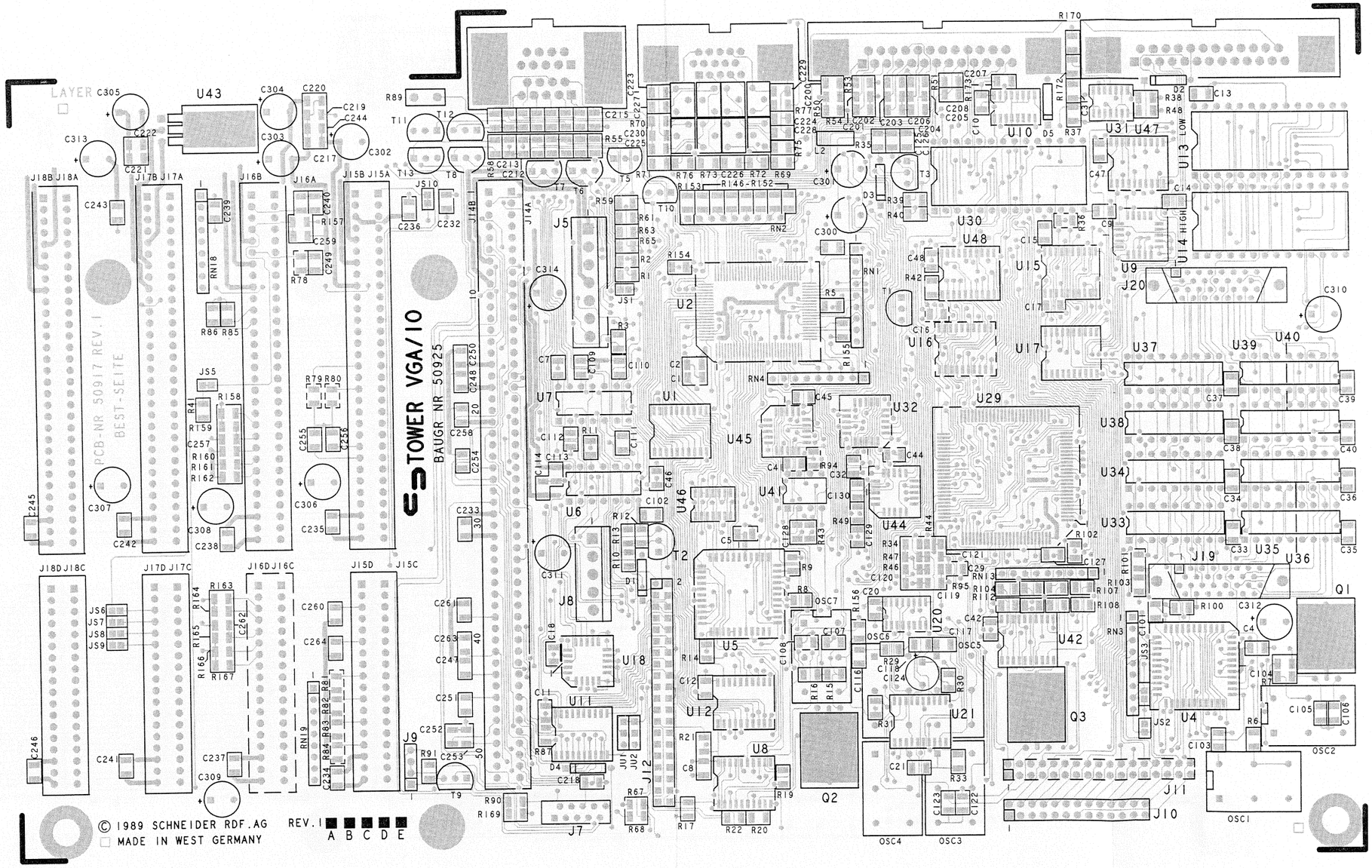
VIO_217

Schneider			
DRAWN BY: K. WINZEK	TITLE: SCHEMATIC TOWER-VGA/IO		
APPROVED:			
USED ON: AT286/386SX	SIZE A 3	50 925	REV 2
DATE: 01-05-90	SHEET: 17 of 19		

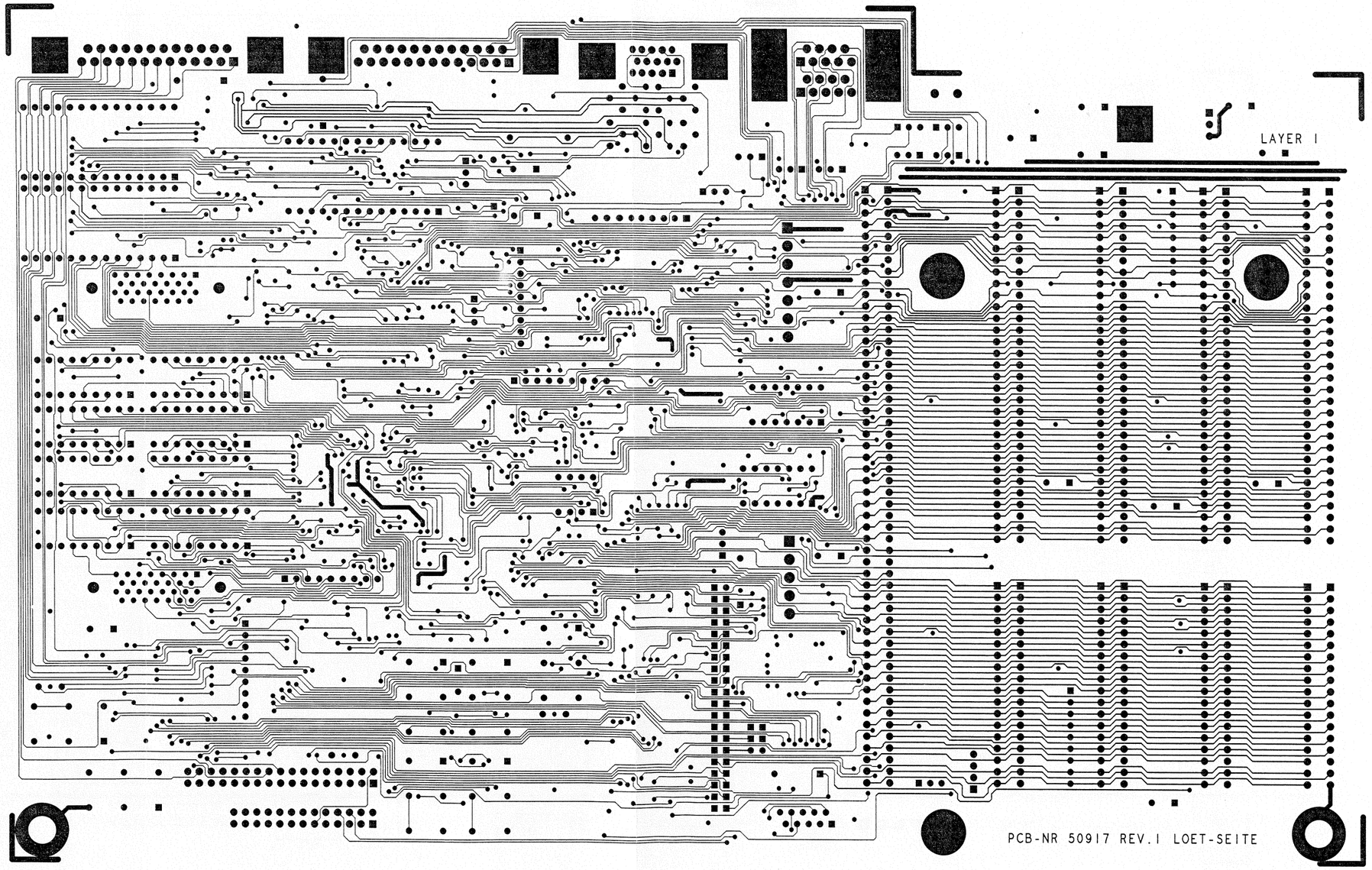

RESETDRV [2-4, 14-17]
SMEMW [6, 14-17]
SMEMR [6, 14-17]
DRQ<0: 3, 5: 7> [3, 14-17, 19]
DACK<0: 3, 5: 7> [2, 14-17]
IRQ<2: 7, 9: 15> [2, 3, 8, 14-17, 19]
MASTER [14-17]
+5V
R85 1K
R86 1K
J18B J18A
J18D J18C
ZEROWS [14-17]
STOW [2, 3, 5, 6, 14-17]
STOR [2, 3, 5, 6, 14-17]
REFRESH [2, 6, 14-17]
SYSCLK [14-17]
TC [3, 14-17]
BALE [5, 14-17]
OSC [14-17]
MEMCS16 [6, 14-17]
IOCS16 [12, 14-17]
+12V
-5V
-12V
IOCHCK [2, 14-17]
SD<0: 15> [2, 3, 5, 6, 14-17]
IOCHRDY [8, 12, 14-17]
SAEN [2, 6, 14-17]
SA<0: 19> [2-6, 8, 14-17]
SBHE [6, 8, 14-17]
LA<17: 23> [6, 14-17]
MEMR [14-17]
MEMW [14-17]
C244 220nF
C245 220nF
C246 220nF
NORMAL SLOT
Schneider
DRAWN BY: K. WINZEK
APPROVED:
TITLE: SCHEMATIC TOWER-VGA/IO
USED ON: AT286/386SX
SIZE A 3
50 925
REV 2
DATE: 01-05-90
SHEET: 18 of 19
V10_218


BLOCK CAPS +5V:
+5V
C309 10uF
C310 10uF
C311 10uF
C312 10uF
C313 10uF
C314 10uF
C1 100nF
C2 220nF
C4 220nF
C5 220nF
C7 220nF
C8 100nF
C9 220nF
C10 100nF
C11 100nF
C12 100nF
C13 100nF
C14 100nF
C15 100nF
C16 100nF
C17 100nF
C18 220nF
C20 100nF
NOTE 1
C21 220nF
C29 220nF
C31 100nF
C32 220nF
C33 220nF
C34 220nF
C35 220nF
C36 220nF
C37 220nF
C38 220nF
C39 220nF
C40 220nF
C41 100nF
C42 100nF
C44 220nF
C45 220nF
C46 100nF
C47 100nF
C48 100nF
SPARE GATES
MC1488
U6/1
N/C
DRQ<0: 3, 5: 7> [3, 14-18]
C247 47pF
C248 47pF
C249 47pF
C250 47pF
C251 47pF
C252 47pF
C253 47pF
IRQ<2: 7, 9: 15> [2, 3, 8, 14-18]
C254 47pF
C255 47pF
C256 47pF
C257 47pF
C258 47pF
C259 47pF
C260 47pF
C261 47pF
C262 47pF
C263 47pF
C264 47pF
NOTES: 1) C211 ONLY INSERTED WITH U21 (PAGE. 7)
VIO 219
Schneider
DRAWN BY: K. WINZEK
APPROVED:
TITLE: SCHEMATIC TOWER-VGA/IO
USED ON: AT286/386SX
SIZE A 3
50 925
REV 2
DATE: 01-05-90
SHEET: 19 of 19

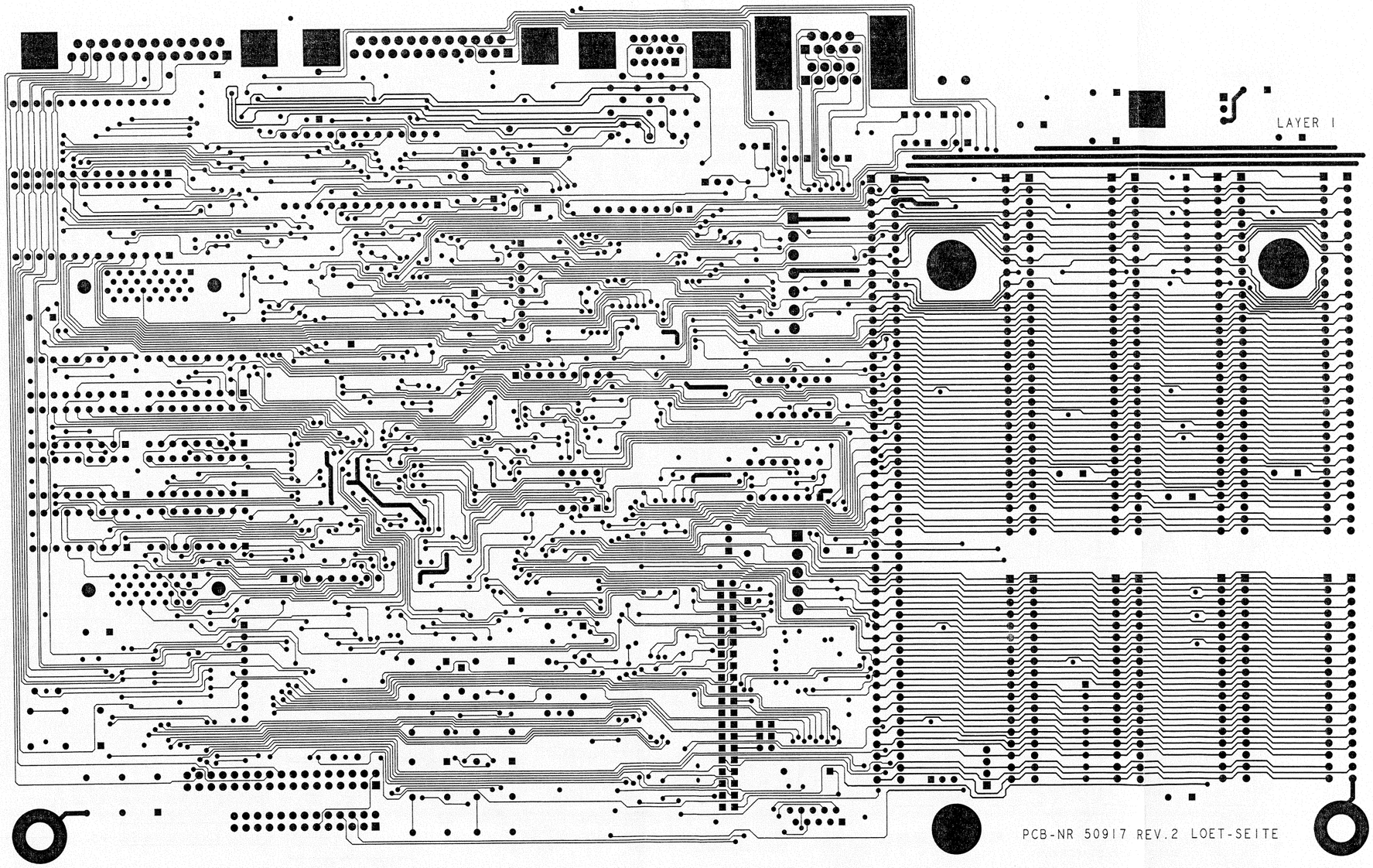
VGA I/0
Component side



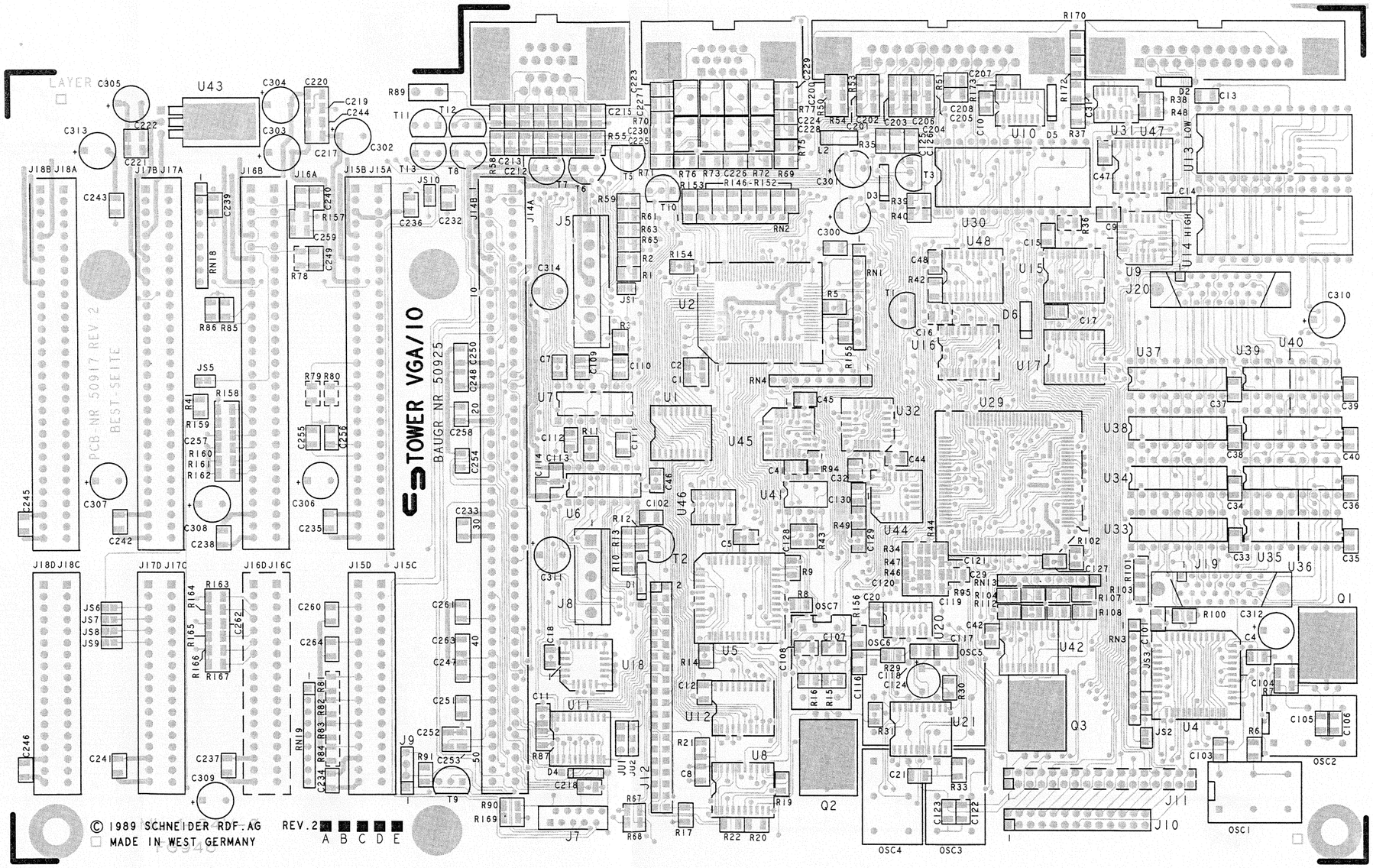
VGA I/0
Soldering side



VGA I/0
Soldering side



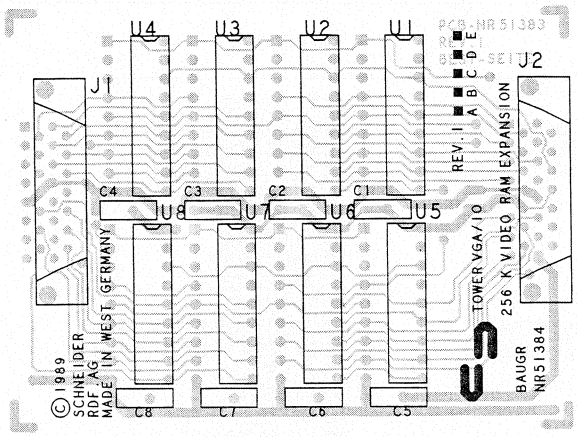
VGA I/0
Component side



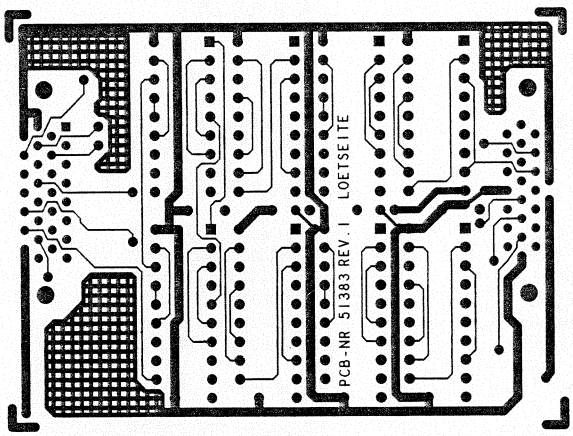
Ersatzteilliste für Platine Best. (D) VGA I/0
Parts List for P.C.B. (D) VGA I/0

Best.-Nr. Part.-No.	Bezeichnung	Description	Zeich.-Pos. Ref.-No.	Preisgruppe
51 319 00	IC 74 LS 245	IC 74 LS 245	U 1	A 7
50 773 00	IC BIG JIM TC110 G008	IC BIG JIM TC 110 G008	U 2	D 1
50 105 00	IC WD 37 C65A-JM00	IC WD 37 C65A-JM00	U 4	D 5
50 827 00	IC 16 C 450 PLCC44	IC 16 C 450 PLCC44	U 5	C 6
50 120 00	IC MC 1488	IC MC 1488	U 6	A 5
50 121 00	IC MC 1489	IC MC 1489	U 7	A 5
51 321 00	IC 74 LS 244	IC 74 LS 244	U 8	B 0
51 546 00	IC PAL 16 L8A	IC PAL 16 L8A	U 9	C 2
51 318 00	IC 74 HC 165	IC 74 HC 165	U 10	A 9
51 319 00	IC 74 LS 245	IC 74 LS 245	U 11, 12	A 7
51 368 00	IC 27C256-15 BIOS »LOW«	IC 27C256-15 BIOS »LOW«	U 13	D 9
51 369 00	IC 27C256-15 BIOS »HIGH«	IC 27C256-15 BIOS »HIGH«	U 14	D 9
51 321 00	IC 74 LS 244	IC 74 LS 244	U 15	B 0
51 319 00	IC 74 LS 245	IC 74 LS 245	U 17	A 7
51 542 00	IC 74 F 151	IC 74 F 151	U 20	A 8
51 377 00	IC ATI 18899-2	IC ATI 18899-2	U 29	F 2
50 955 00	IC G176P-50	IC G176P-50	U 30	D 2
51 543 00	IC LM 339	IC LM 339	U 31	B 2
51 378 00	IC PAL 16 L8A	IC PAL 16 L8A	U 32	C 2
50 118 00	IC DRAM 64K×4	IC DRAM 64K×4	U 33–40	C 7
51 326 00	IC NMC 930 6N	IC NMC 930 6N	U 41	B 2
50 933 00	IC 74 F 241	IC 74 F 241	U 42	A 8
50 238 00	IC 7905 T0220	IC 7905 T0220	U 43	A 6
51 423 00	IC PAL 16 L8B	IC PAL 16 L8B	U 44	C 2
51 422 00	IC PAL 16 L8A	IC PAL 16 L8A	U 45	C 2
51 545 00	IC 74 F 32	IC 74 F 32	U 46	A 5
51 321 00	IC 74 LS 244	IC 74 LS 244	U 47	B 0
51 319 00	IC 74 LS 245	IC 74 LS 245	U 48	A 7
50 338 00	Diode 1 N 4148	Diode 1 N 4148	D 1–5	A 0
52 167 00	Diode SB 120	Diode SB 120	D 6	A 3
50 358 00	Transistor BC 337 B	Transistor BC 337 B	T 1–3, 5–8	A 2
51 042 00	Transistor BC 327 B	Transistor BC 327 B	T 9–13	A 2
51 093 00	Quarz 9,6 MHz	Crystal 9.6 MHz	Q 1	A 8
50 313 00	Oszillator 16,0 MHz	Oscillator 16,0 MHz	OSC 1	C 0
50 990 00	Oszillator 50,0 MHz	Oscillator 50.0 MHz	OSC 3	B 9
50 989 00	Oszillator 45,0 MHz	Oscillator 45.0 MHz	OSC 4	B 9
50 988 00	Oszillator 36,0 MHz	Oscillator 36.0 MHz	OSC 5	B 9
50 991 00	Oszillator 56,644 MHz	Oscillator 56.644 MHz	OSC 6	B 9
51 330 00	Oszillator 1,8432 MHz	Oscillator 1.8432 MHz	OSC 7	C 2
51 332 00	Spule-HF 4,7 uH	Coil, HF 4.7 uH	L 2	A 5
50 321 00	Widerstand PTC OR 75	Resistor PTC OR 75	R 89	B 0
50 316 00	R-Netzwerk 8×10K	R-Network 8×10K	RN 1	A 3
50 317 00	R-Netzwerk 8×1K0	R-Network 8×1K0	RN 2, 3	A 3
50 319 00	R-Netzwerk 8×4K7	R-Network 8×4K7	RN 4, 13, 18, 19	A 3
50 133 00	Buchse SUB-D 25pol.	Socket SUB-D 25-pin	J 1, 6	B 2
50 949 00	Buchse SUB-D 9pol.	Socket SUB-D 9-pin	(J 2 + 4)	C 3
50 254 00	Stiftleiste RM 3,96 7pol.	Connector RM 3.96 7-pin	J 5	A 5
51 375 00	Stiftleiste RM 1,27 10pol.	Connector RM 1.27 10-pin	J 7	A 3
50 322 00	Stiftleiste RM 3,96 5pol.	Connector RM 3.96 5-pin	J 8	A 3
51 376 00	Stiftleiste RM 2,54 1×5pol.	Connector 2.54 1×4-pin	J 9	A 1
51 569 00	Stiftleiste RM 2,54 26pol.	Connector 2.54 26-pin	J 10	A 7
51 085 00	Stiftleiste 2×20	Connector 2×20	J 12	A 7

Option VGA/RAM-Modul
Component side



Soldering side



Ersatzteilliste für VGA/RAM-Modul
Parts List for VGA/RAM-Modul

Best.-Nr. Part.-No.	Bezeichnung	Description	Zeich.-Pos. Ref.-No.	Preisgruppe
51 384 00	VGA/RAM-Modul	VGA/RAM-Modul		F 7
50 118 00	IC 41464-10 DRAM 64 K×4 100nS	IC 41464-10 DRAM 64 K×4 100nS	U 1–8	C 7
51 519 00	Steckverb. CHAMP 30pol.	Socket CHAMP 30-pin		B 2

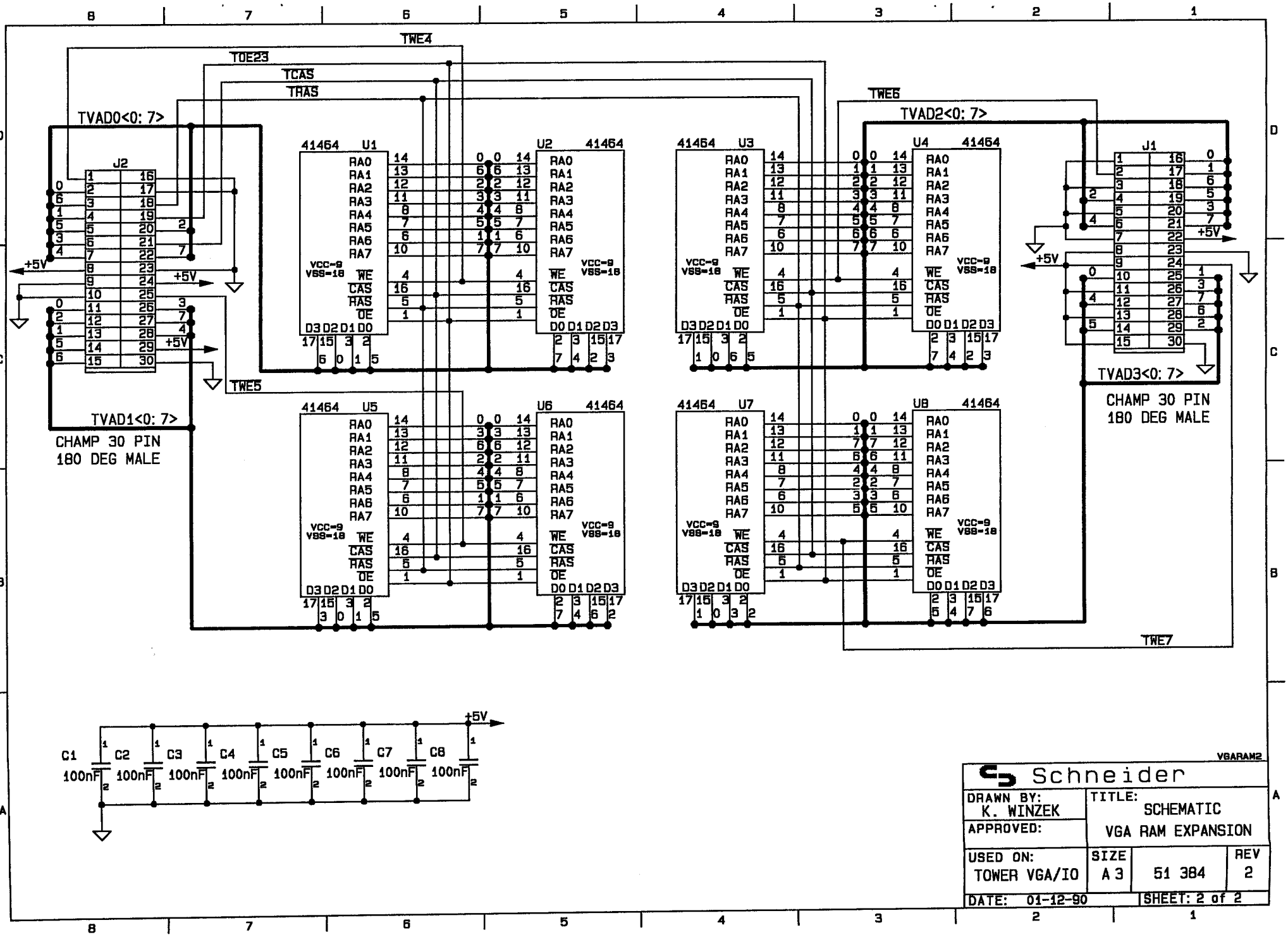
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
1	ADVANCED ENGINEERING RELEASE	07-17-89	
2	NEW RAM MODUL CONNECTORS (PCB REV.1)	01-10-90	K. WINZEK

DRAWING FILES:	CONTENTS:
VGARAM1.DWG	THIS SHEET
VGARAM2.DWG	VGA RAM EXPANSION

VGARAM1

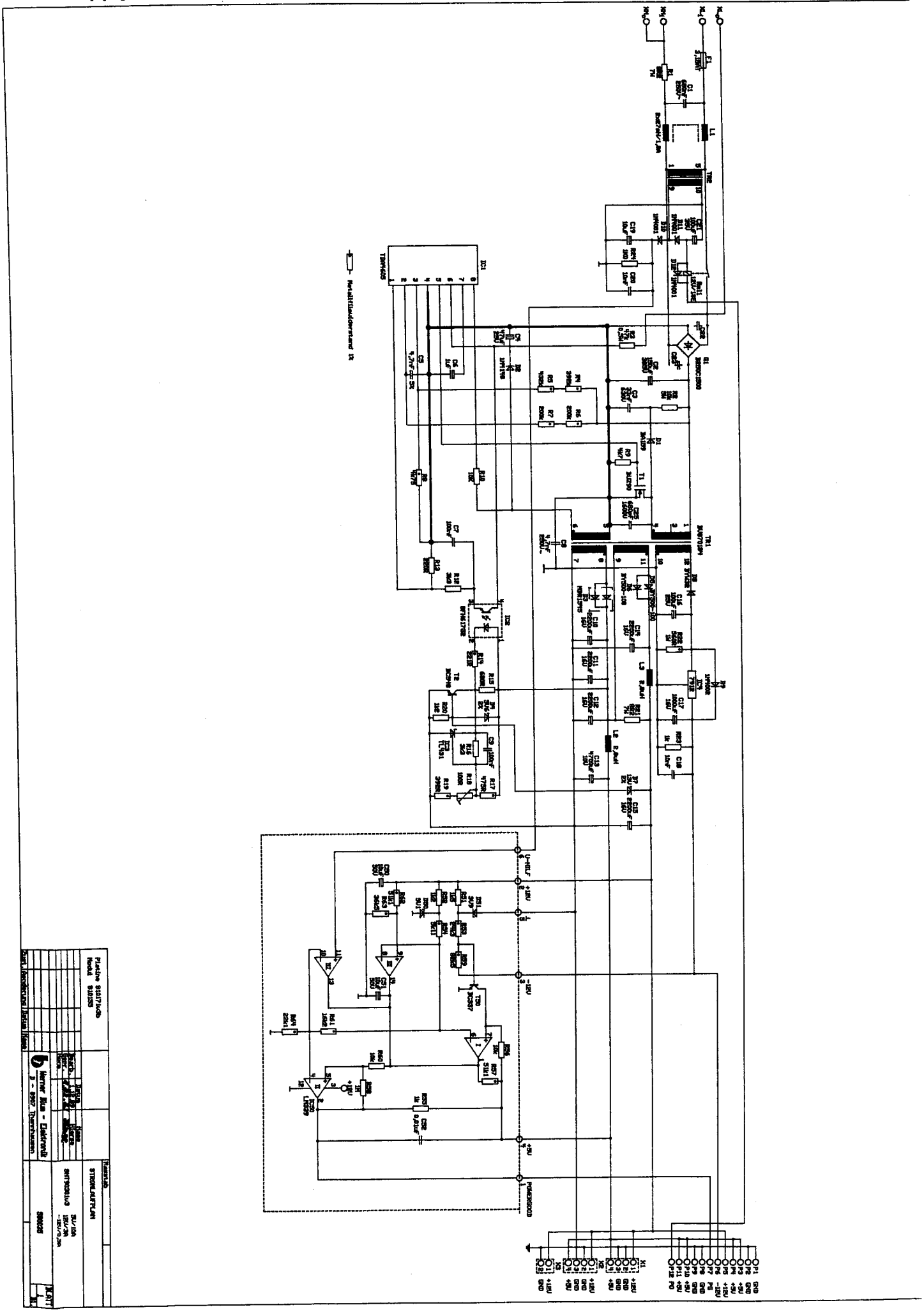
Schneider

DRAWN BY: K. WINZEK	TITLE: SCHEMATIC VGA RAM EXPANSION		
APPROVED:			
USED ON: TOWER VGA/IO	SIZE A 3	51 384	REV 2
DATE: 01-12-90	SHEET: 1 of 2		



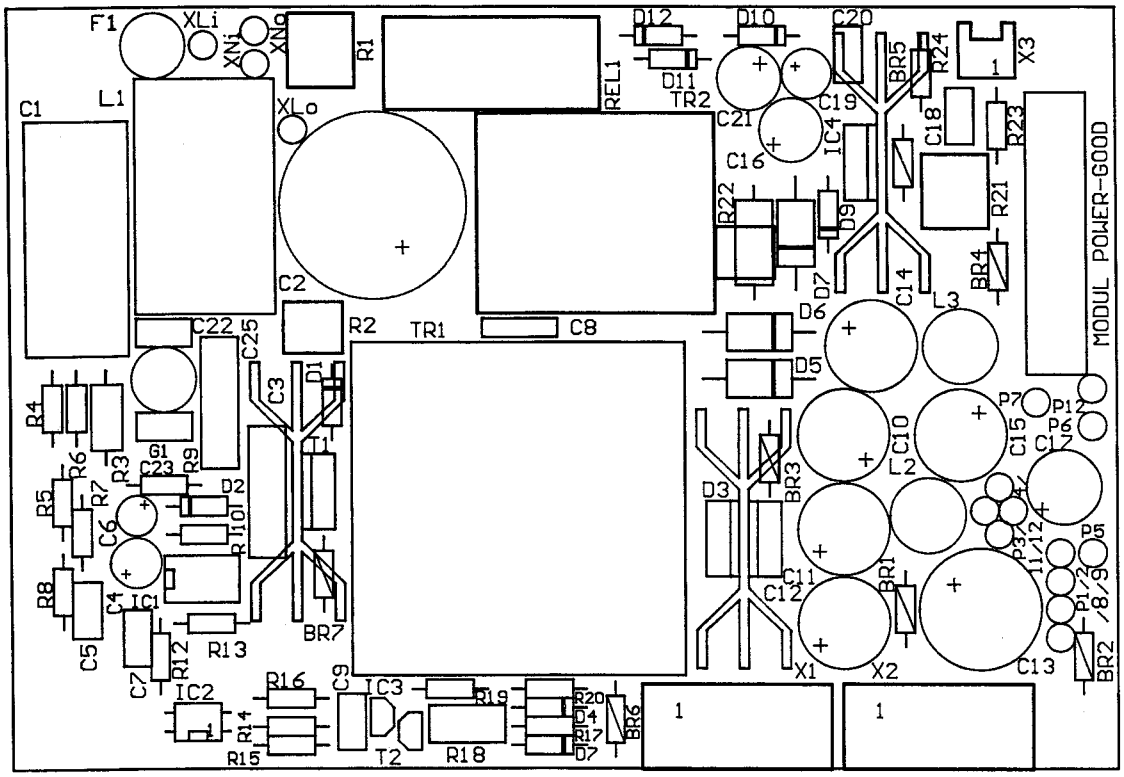
Schneider			VGARAM2
DRAWN BY: K. WINZEK	TITLE: SCHEMATIC VGA RAM EXPANSION		
APPROVED:			
USED ON: TOWER VGA/IO	SIZE A 3	51 384	REV 2
DATE: 01-12-90	SHEET: 2 of 2		

Schematic diagram
Power supply



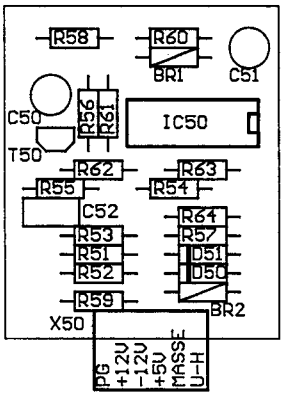
Power supply
Component side

SNT90301 Fa. Schneider
Ident.-Nr.: 810171V3b
Groesse: 149,5*103mm



Modul
Power supply

Modul Power-Good fuer SNT 60301/90301
Ident.-Nr.: 810155
Groesse: 38*45 mm



1. Product definition

General:

The CPU card is a IBM AT-class dual speed compatible machine operating at 8 and 16 MHz. Unlike the IBM PC/AT, the clocks used for the CPU and AT bus may be synchronous or asynchronous. The Chips & Technology's CS8281 CHIPSet is used for reduced parts count and cost. With this layout removing the entire CPU becomes as easy as removing an option card, simplifying maintenance and upgrades.

Fast A20 gate switching and EMS are incorporated for improved performance for DOS utilities, respectively.

Features:

- Fully IBM compatible.
- 16 MHz CPU speed, operating with 0 wait states.
- Socket for 16 MHz Intel 80387SX Math Coprocessor.
- Separate CPU and AT bus clocks.
- 1 MB on-board parity checked RAM minimum; expandable to 5 MB on-board maximum.
- Shadowing capability for BIOS and Video ROM.
- EMS memory support.
- 8 MHz AT bus.
- Supports 16 MHz operation with only 0.3 –0.7 wait states for 100ns DRAMs.
- Page interleaved memory access.
- Schneider enhanced, Phoenix ROM BIOS.
- Fast A20 gate switching.

2. Architecture

This board is a new generation of an AT compatible CPU board which works at 16 MHz while still using low cost slow memories. 386SX CPU Board maintains full compatibility with IBM PC/AT. Additionally, it supports the Expanded Memory Specification (EMS) memory, extended memory, and advanced memory paging schemes for on-board memory up to 5 Mbyte. Since it is manufactured using CMOS technology, CS8281 chipset consume about one third of the power of its TTL counter parts. 386SX CPU Board supports both the MS-DOS and OS/2 operating systems. It supports the built-in FAST GATE A 20 and FAST CPU RESET which allow the fast switching between the real address mode and protected mode. This feature will improve the OS/2 performance up to 20 % over conventional chipsets which will run OS/2. Due to shadowing of BIOS and Video ROM, system performance will not be degraded by the slow access speed of EPROM. However, unlike the IBM PC/AT, the clocks used for the CPU and AT bus may be asynchronous or synchronous. This arrangement allows for a greater flexibility in the system design and yields higher performance and yet, maintains the PC/AT compatibility. In either mode, the CPU can operate at high clock speeds, however, the clock source for the AT bus (ATCLK) is different.

An Intel 8742 peripheral controller performs all the keyboard interfacing as well as conventional A20 gate switching and hot reset. The 8742 controller has 128 bytes of data memory, and 2 Kbytes of program memory containing Phoenix Compatibility software. Included in this architecture are 7 DMA channels, 13 interrupt request channels, 2 counter/timer channels, and real time clock in 82C206. Configuration information is contained in 114 bytes of CMOS RAM memory. Both the real time clock and configuration RAM are battery backed up CMOS for continuous operation.

The block diagram in Figure 1 demonstrates the functional layout of the 386SX CPU Board design. The 82C811 Bus controller performs all the bus sizing and flow control for the system. There are four buses supported by the CS8281 chipset as shown in Figure 1: CPU local bus (A and D), system memory bus (MA and MD), I/O channel bus (SA and SD), and X bus (XA and XD). The system memory bus is used to interface the CPU to the DRAMs and EPROMs controlled by the 82C812. The I/O channel bus refers to the bus supporting the AT bus adapters which could be either 8 bit or 16 bit devices. The X bus refers to the peripheral bus to which the 82C206 IPC and other peripherals are attached in an IBM PC/AT.

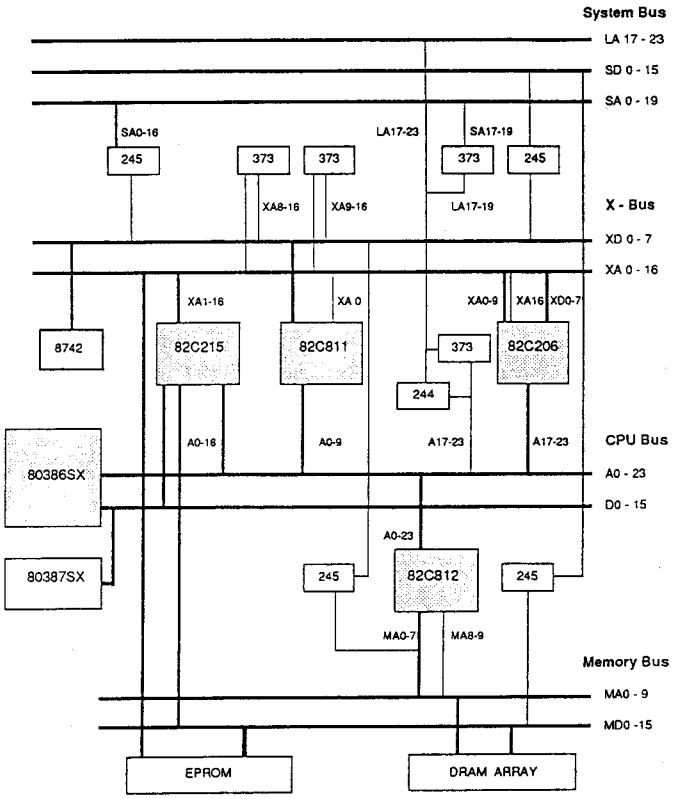


Figure 1. 386SX CPU Board Block Diagram

The 82C811 provides a flexible clock selection scheme as shown in Figure 2. It has two input clocks; CLK2IN and ATCLK. CLK2IN is driven from a TTL crystal oscillator, running at a maximum of twice the processor clock (PROCCLK) frequency. ATCLK is derived from a crystal. Typically, it should be of a lower frequency than CLK2IN. ATCLK and CLK2IN can be selected under program control. The 82C811 generates processor clock, PROCCLK, for driving the CPU state machine and interface. SCLK (internal) is the AT bus state machine clock and is used for the AT bus interface.

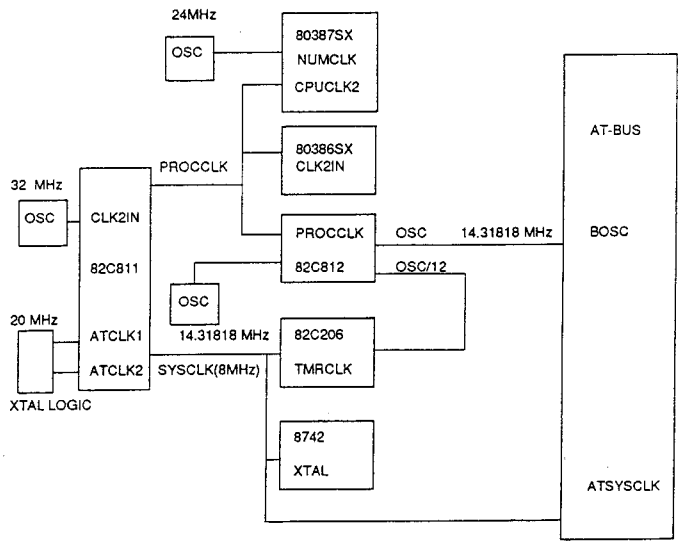


Figure 2. 386SX Frequency Path & Block Diagram

3. Detailed description

3.1 80386SX Micro processor

The 80386SX combines a full 32 bit internal architecture with a 16 bit external data bus and 24 bit external address bus. This provides the performance benefits of a 32 bit programing architecture while taking advantage of the cost savings associated with 16 bit systems. The 80386SX will operate at zero wait states. Zero wait states are obtainable by using 100ns access time DRAMs.

3.2 80387SX Coprocessor

A socket is provided, and all support circuitry implemented on the Processor Board to direcly accept an Intel 80387SX Coprocessor chip operating at 16 MHz. No switch settings are necessary for the system to recognize the Coprocessor at 16 MHz. A one jumper change will allow the 80387Sx to operate at 12 MHz (Asynchronous Mode) for backward compatibility. This jumper information is described in section 4.3.

3.3 82C811 CPU/BUS Controller

The 82C811 provides the following functions:

- Reset and Shutdown logic.
- Clock generation with software speed selection.
- Optional independent AT bus clock.
- CPU interface and Bus control.
- Port B register.
- Coprocessor interface logic.
- Refresh logic.
- Programmable command delays and wait state generation.

82C811 generates memory refresh signal, refresh addresses, interface lines to and from CPU and Coprocessor and control signals for the peripheral devices and AT bus. 82C811 includes the AT bus state machine, CPU state machine, reset/shutdown logic, bus arbitration/refresh logic and other interface circuitry. At the beginning of a cycle 82C811 samples AF16 from 82C812 to determine whether the current cycle is the local memory cycle I/O or AT bus cycle. If the cycle is a local memory cycle (AF16 is asserted), i.e.a local memory read or write, the 82C811 just waits and monitors the READY signal from 82C812 to complete the current cycle. 82C812 will generate READY signal to the CPU at the end of the current cycle. If the bus cycle is not a local memory read/write cycle (AF16 is not asserted), 82C811's AT bus state machine will be started. It will issue AT bus memory or I/O read/write command, ACEN (action code enable), AC0/1 (Action – Code control lines) and other bus required control signals. It will also issue READY at the end of the current AT bus or I/O cycle.

3.4 82C812 Memory interleave/page controller

The 82C812 provides the following functions:

- Page mode access, providing higher performance.
- Supports 100ns DRAMS at 16 MHz (page interleaved mode).
- Shadow RAM.
- OS/2 optimization.
- Automatic memory remapping.
- Supports EMS.

82C812 generates the timing signals (RAS, CAS, MA addresses, WE, etc.) needed to access the system base memory (0-640 KB), EPROM, the EMS memory. Through the memory mapping logic, for up to 1 MB of system RAM, it is possible to map RAM that overlaps the EPROM area above the 1 MB area. Hence, for 1 MB of on board RAM, the software can address it from 0 to 640 KB and from 1 MB to 1.384 MBs. 82C812 provides an interleaved memory subsystem design with page mode operation. It supports up to 5 MB of DRAM with the combinations of 256 KB and 1 MB DRAMs. The processor can operate at 16 MHz with 0.7 wait state memory accesses, using 100 ns DRAMs. This is possible through a page interleaved memory scheme. A RAM shadowing feature allows faster executions of EPROM stored BIOS code by down-loading and executing code from RAM.

Two way access methods permit larger zero wait state hit space. Table 1 shows all the possible memory configurations for the CS8281 CHIPset.

EMS Address Translational Logic

The 82C812 provides mapping hardware that is compatible with the Expanded Memory Specification, version 3.2 (EMS 3.2). This allows a 64K block of address (C0000H-EFFFFH) to be used as a window (called a page frame) into a larger memory map. The page frame is divided into four 16K blocks (pages) that can be independently redirected to any area within the 82C812's memory map (but not to locations on the AT bus). The EMS specification allows the processor to access to the vast amounts of memory while remaining in real address mode.

3.5 82C215 Data/address buffer

The 82C215 performs the following functions:

- Address buffers and latches.
- Data buffers and latches.
- Bus conversion logic.
- Party generation/detection logic.

82C215 provides the bi-directional address and data buffers between the CPU and the peripherals. It also performs bus conversion of 16 bit I/O or memory read/write for an 8 bit I/O or memory add-on card according to the action code signals coming from 82C811 (AC0, AC1, ACEN). The 82C215 will also provide the parity generation and detection logic for the local memory read/write. The parity error (PARERR) and I/O channel parity error (IOCHCK) from AT bus will be directed to 82C811 to generate NMI (Non-Maskable Interrupt), if the NMI parity error check and I/O channel check bits of Port B (I/O port 61 h) are enabled. The parity error is ignored in EPROM access cycles. 82C811 polls the ROMCS signal from 82C812 to determine whether the current local memory cycle is an EPROM cycle or not.

3.6 82C206 integrated peripherals controller

- Fully compatible to Intel's 8237 DMA controller, 8259 Interrupt controller, 8254 Timer/Counter, and Motorola's 146818 Real Time Clock.
- Offers 7 DMA channels, 13 Interrupt request channels, 2 Timer/Counter channels, and a Real Time Clock.
- Reduced recovery time (120 ns) between control.
- 114 bytes of CMOS RAM memory.
- 8 MHz DMA clock with programmable internal divider for 4 MHz operation.
- Programmable wait states for the DMA cycle.
- 16 Mbytes DMA address space.
- Single chip 84-pin CMOS implementation.

The 82C206 is a LSI implementation of the standard peripherals required to implement an IBM PC/AT system board. This device contains the equivalent of two 8237 A DMA Controllers, a 74LS612 Mapper, two 8259A Interrupt Controllers, and 8254 Counter/Timer, and a MC146818 Real Time Clock with RAM. The 82C206 provides all of the standard peripherals required for a system board implementation except the keyboard interface controller. Two DMA Controllers are provided and connected in such a way as to provide the user with four channels of DMA (DMA1) for 8-bit transfers and three channels of DMA (DMA2) for 16-bit transfers (the first 16-bit DMA channel is used for cascading). Included as part of the DMA subsystem is the Page Register (DMAPAGE) device which is used to supplement the DMA and drive the upper address lines when required. Sixteen channels of interrupt are provided in the 82C206. These channels are partitioned into two cascaded controllers (INTC1, INTC2) with 8 inputs each. Of these 16 channels, three are connected internally to various devices, allowing 13 user definable channels of interrupt. The three internally connected channels are as follows:

Channel 0 – Counter/Timer Counter 0 Interrupt.
Channel 2 – Cascade to Slave Interrupt Controller (INTC2)
Channel 8 – Real Time Clock Interrupt.

The remaining 13 channels may be defined and utilized as necessary to meet the user specific system requirements.

A Counter/Timer (CTC) subsystem is provided which contains three independent counters. All three counters are driven from a clock input pin which is independent from the other clock inputs to the device. Counter 0 is connected to Interrupt 0 of INTC1. It is intended to be used as a multi-level interrupt to the system for such tasks as time keeping and taskswitching. Counter 1 may be programmed to generate pulses or square waves for use by external devices. The third channel (Counter 2) is a full function Counter/Timer which has a gate input for controlling the internal counter. This channel can be used as an interval counter, a timer, or as a gated rate/pulse generator.

A Real Time Clock (RTC) is included in the 82C206 for maintaining the time and date.

This subsystem also contains 114 bytes of RAM in addition to the Clock/Calendar. The Clock/Calendar information and RAM are kept active by connecting the device to an external battery when system power is turned off.

Table 1. Memory Specification

	DRAM Type				Total Memory
	Bank0	Bank1	Bank2	Bank3	
1	256K	256K	0	0	1MB
2	256K	256K	256K	256K	2MB
3	256K	256K	1MB	1MB	5MB

4. Configurations

4.1 Jumpers

The 386SX CPU Board affords many user configured options. The following are the options and their recommended configurations.

Jumper	Pins	Default	Descriptions
E1	1-2	1-2	64KB(27256) ROM select
	2-3		128KB(27512) ROM select
E3	1-2	1-2	CLKM is strapped to Vcc: The math coprocessor operates synchronously with respect to the CPU
	2-3		CLKM is strapped to GND: The NPX operates in asynchronous mode
E4	No jumper		Disconnect -NA of 80386SX from GND: Disable Pipeline mode in the CPU
	1-2	1-2	Connection of -NA to GND: Support Pipeline mode in the CPU
E5	1-2	1-2	Color monitor selection
	2-3		Monochrome monitor selection
E6	No jumper	No jumper	MAN JMP disable
	1-2		MAN JMP enable (for diagnostic usage) POST looping test

A schematic diagram in Figure 3, shows jumper locations and other components. Missing jumpers can be neglected.

4.2 Memory

Small card called Single Inline Memory Module (SIMMs) installed in sockets on the CPU card provide onboard RAM. Each SIMM contains nine memory chips, and provides either 256 KB or 1 MB of memory.

The system supports three types of SIMM modes: static column RAM, fast-paged mode RAM, and standard RAS/CAS RAM. Page mode RAM is pre-installed in the system.

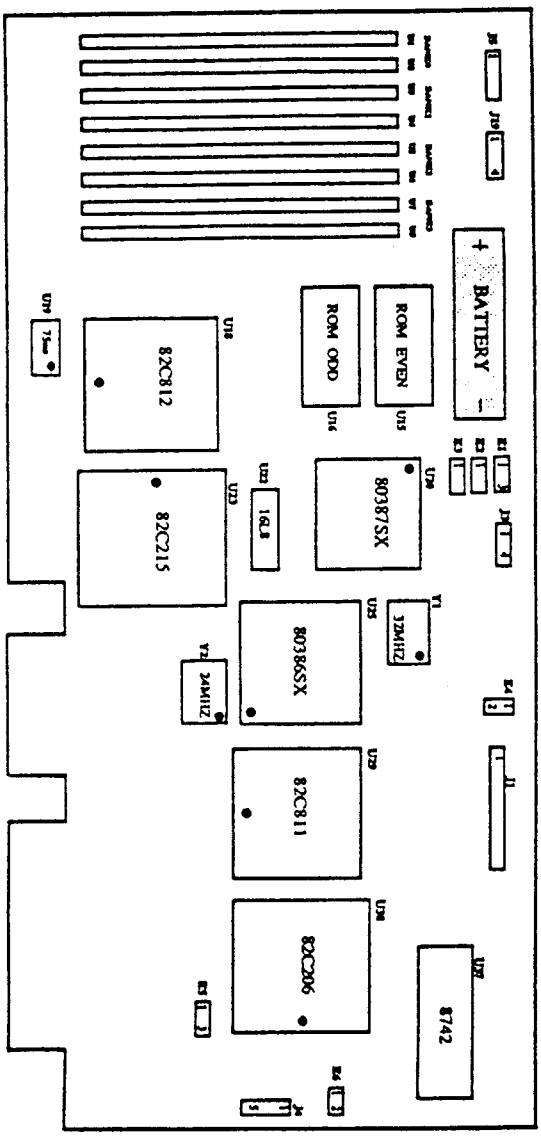


Figure 3. Major Components and Jumper Locations

4.3 Further informations about jumpers

1) ROM Size, E1

The 64 Kbyte ROMs installed in the unit consist of two 27256 chips. These can be replaced by two 27512 chips for a total of 128 kbytes of ROM.

ROM Size	Jumper Pin Setting
64K	Pin 1 and 2 of E1
128K	Pin 2 and 3 of E1

2) Numeric Coproccessor Clocking Mode, E3

When clocking Mode (CLM) pin is strapped to Vcc (High), the numeric coprocessor operates in synchronous mode, when strapped to Vss (Low), the NPX operates in asynchronous mode. These modes relate to clocking of data interface and control unit and the floating-point unit only; the bus controller logic always operates synchronously with respect to CPU.

Condition	Jumper Pin Setting
CLM strapped to Vcc	Pin 1 and 2 of E3
CLM strapped to Vss	Pin 2 and 3 of E3

3) 80386SX Next Address Request (Pipelining), E4

This is used to request address pipelining. Address pipelining indicates the system is prepared to accept new values even if the end of the currant cycle is not being acknowledged. If this input is active (active low) when sampled, the next address is driven onto the bus, provided the next bus request is already pending internally. Pipelined address gives access to three more bus states.

Condition	Jumper Pin Setting
Address Pipelining Enable	Pin 1 and 2 of E4
Address Pipelining Disable	No Jumpers

4) Monitor Type

The factory default setting is a color monitor; however, specifying the monitor type does not take into account the monitor controller type. Ensure that the type of monitor (color or monochrome) is compatible with the monitor controller. The setup program is used to specify the type of monitor controller.

Monitor Type	Jumper Pin Setting
Color	Pin 1 and 2 of E5
Monochrome	Pin 2 and 3 of E5

5) 8742 POST Looping Test

This jumper is only for factory diagnostic usage, and is not user configurable.

Condition	Jumper Pin Setting
Test Enable	Pin 1 and 2 of E6
Test Disable	No Jumpers

5. Connectors

These are the keyboard, speaker, and front panel connectors.

5.1 J1, System Power Interface

Pin	Signal
1	LEDPWR
2	-KBDINH
3	-RETSW
4	GND
5	SPKRF
6	PWRGD
7	KBDPWRF
8	KBDGNDF
9	KBDDATF
10	KBDCLKF

5.2 J3, Battery Interface

Pin	Signal
1	+ 3.6V (BATT)
2	N.C
3	GND
4	GND

5.3 J4, Keyboard Interface

Pin	Signal
1	KBDCLKF
2	KBDDATF
3	N.C
4	KBDGNDF
5	KBDPWRF

5.4 J5, Keylock Interface

Pin	Signal
1	LEDPWR
2	N.C
3	GND
4	-KBDINH
5	-RSTSW

6. System bus connectors

The System Bus Connectors consist of all the necessary signals needed to connect the CPU to the expansion bus. These are two gold fingered edge connectors, P1 and P2. P1 is the traditional 8-bit IBM XT compatible bus, while P2 makes up the IBM XT compatible 16-bit extension bus.

6. P1

A01 – -IOCHCK	A02 – SD07	A03 – SD06
A04 – SD05	A05 – SD04	A06 – SD03
A07 – SD02	A08 – SD01	A09 – SD00
A10 – IOCHRDY	A11 – AEN	A12 – SA19
A13 – SA18	A14 – SA17	A15 – SA16
A16 – SA15	A17 – SA14	A18 – SA13
A19 – SA12	A20 – SA11	A21 – SA10
A22 – SA09	A23 – SA08	A24 – SA07
A25 – SA06	A26 – SA05	A27 – SA04
A28 – SA01	A29 – SA02	A30 – SA0
A31 – SA00		
B01 – GND	B02 – RESETDRV	B03 – VCC
B04 – IRQ09	B05 – N.C.	B06 – DREQ2
B07 – N.C.	B08 – 0WS	B09 – N.C.
B10 – GND	B11 – SMEMWOUT	B12 – SMEMROUT
B13 – -IOW	B02 – IOR	B15 – -DACK3
B16 – DREQ3	B17 – DACK1	B18 – DREQ1
B19 – -REF	B20 – SYSCLK	B21 – IRQ07
B22 – IRQ06	B23 – IRQ05	B24 – IRQ04
B25 – IRQ03	B26 – DACK2	B27 – TC
B28 – BALE	B29 – VCC	B30 – OCS
B31 – GND		

6.2 P2

C01 – SBHE	C02 – LA23	C03 – LA22
C04 – LA21	C05 – LA20	C06 – LA19
C07 – LA18	C08 – LA18	C09 – -MEMR
C10 – -MEMW	C11 – SD08	C12 – SD09
C13 – SD10	C14 – SD11	C15 – SD12
C16 – SD13	C17 – SD14	C18 – SD15
D01 – -MEMCS16	D02 – IOCS16	D03 – IRQ10
D04 – IRQ11	D05 – IRQ12	D06 – IRQ15
D07 – IRQ14	D08 – -DACK0	D09 – DREQ0
D10 – -DACK5	D11 – DREQ5	D12 – -DREQ6
D13 – DREQ6	D14 – -DACK7	D15 – DREQ7
D16 – +5 VDC	D17 – MASTER	D18 – GND

********* **ACHTUNG!** *********

Für Daten aller Art, die sich bei Einsendung an die Firma Schneider im Servicefall oder in jedem anderen Fall noch auf einem Datenträger befinden, wird bei Verlust oder Beschädigung keinerlei Haftung übernommen!
Bitte, sichern Sie sich Ihre Daten vorher von Ihrem Datenträger. Wie man eine Sicherungskopie erstellt, können Sie in Ihrer MS-DOS-Betriebsanleitung nachlesen.

********* **IMPORTANT!** *********

We accept no responsibility for the loss of or damage to data of any kind which is still contained on a data carrier which is sent to Schneider for servicing or for any other reason!
Please copy your data from your data carrier beforehand. You can read how to produce a backup copy in your MS-DOS operating instructions.

Bitte bei Ersatzteilbestellung die genaue Bezeichnung und Ident-Nr. (siehe Typenschild) des Gerätes sowie Bestell-Nummer und Positions-Nummer des Ersatzteils angeben.

For ordering of spare parts please state exact description and ident.-no. of unit (see silver rating label on the backside of unit) as well as part-no. and position-no. of required spare parts.

Benutzen Sie:

Telex: 531516

oder

*317298 #

oder

Telefax: 08245/51326